Stanford University

EE101B
Circuits II

Spring 2017
Boris Murmann

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Chapter 1

Introduction

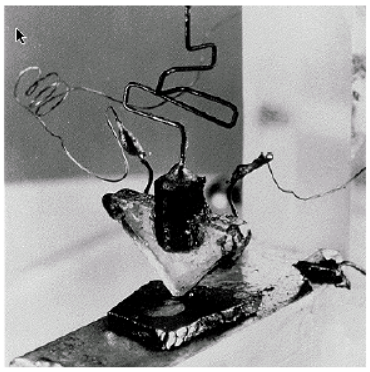
Boris Murmann

Stanford University

Circuits are Everywhere!

The Beginning

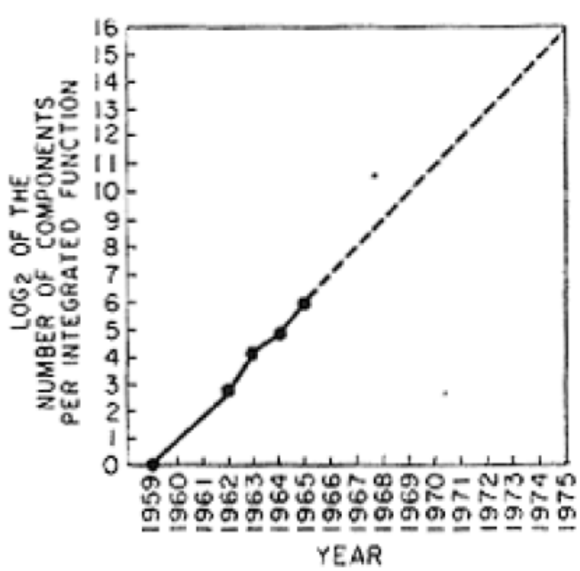
Transistor
Bardeen, Brattain, Shockley, 1948



Integrated Circuit
Kilby, 1958

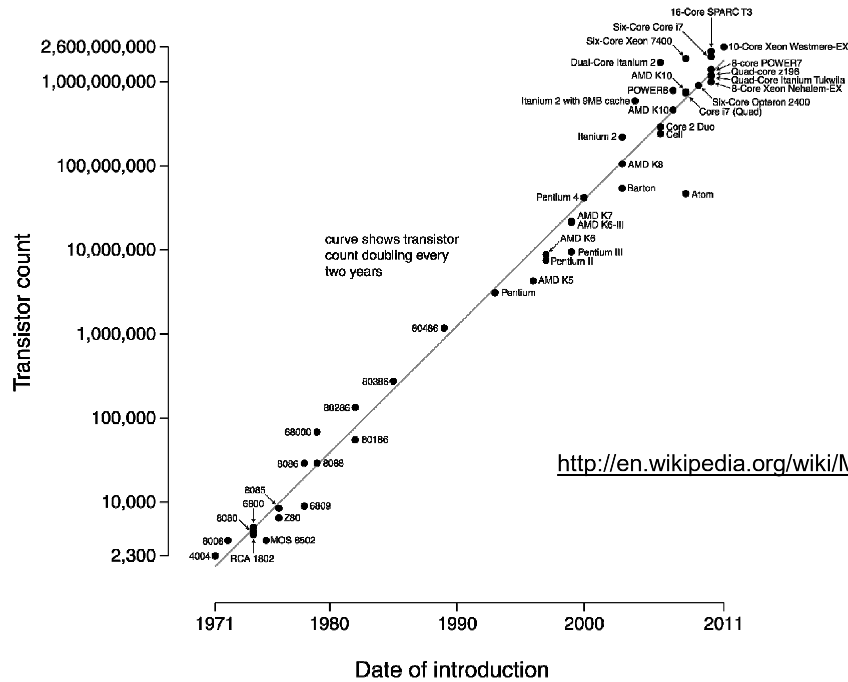
Moore's Law

- In 1965, Gordon Moore predicted exponential growth in the number of transistors per integrated circuit



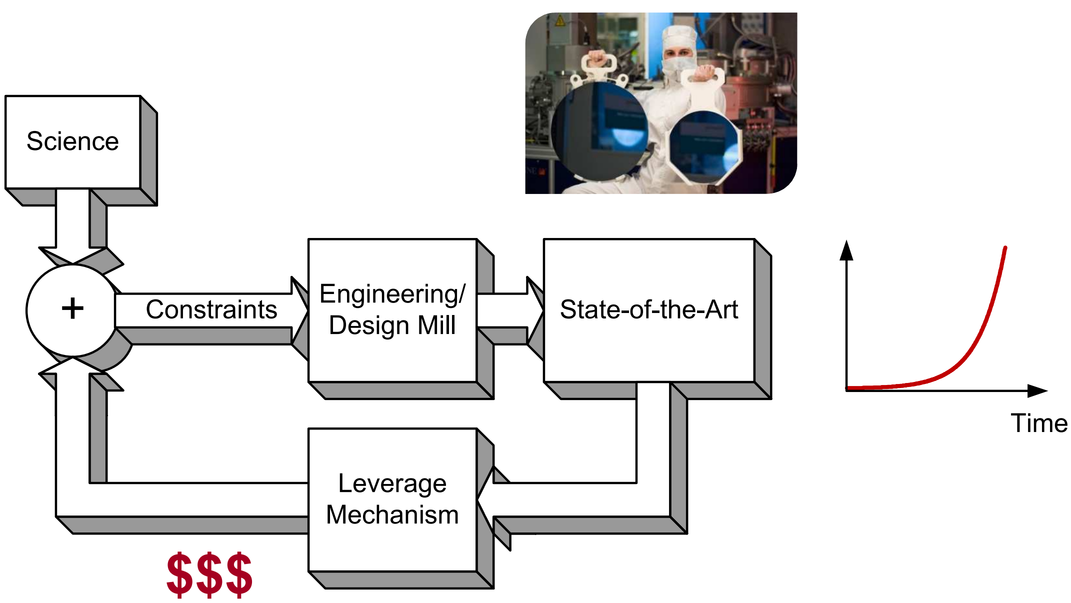
… And He was Right

Microprocessor Transistor Counts 1971-2011 & Moore's Law



http://en.wikipedia.org/wiki/Moore's_law

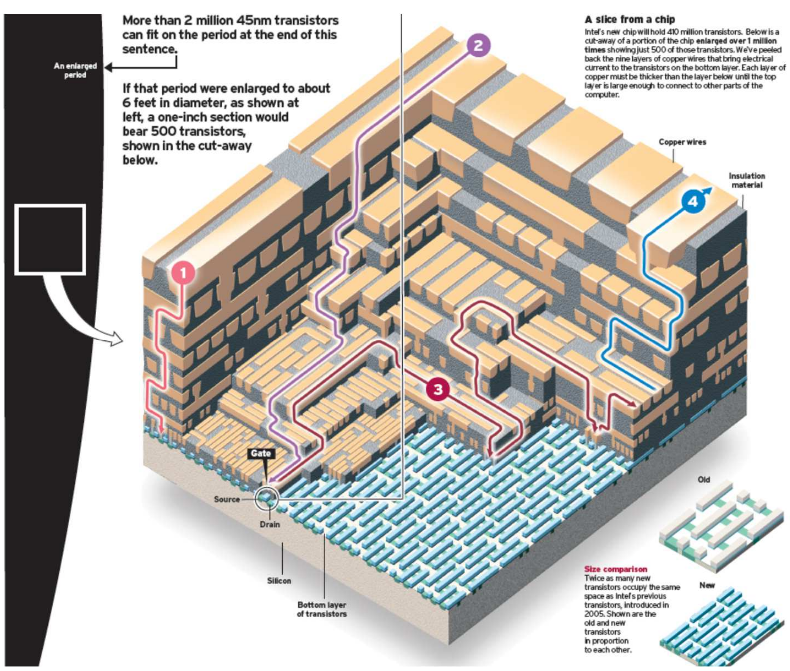
A Gigantic (Economic) Feedback Loop



State-of-the-Art Semiconductor Fab

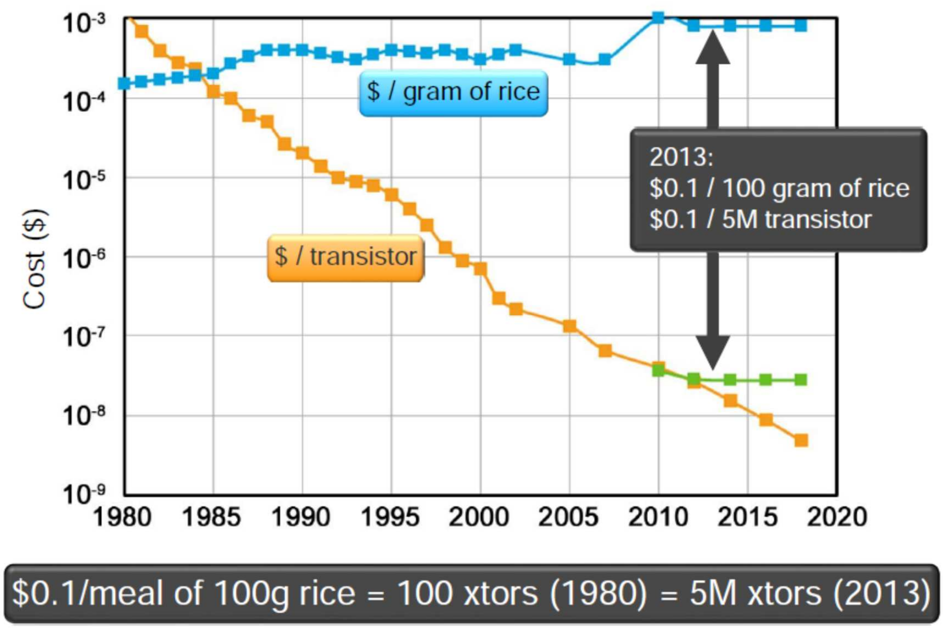
Intel's "Fab 32" (Chandler, Arizona) ~ $3 Billion

45nm Technology (Intel)



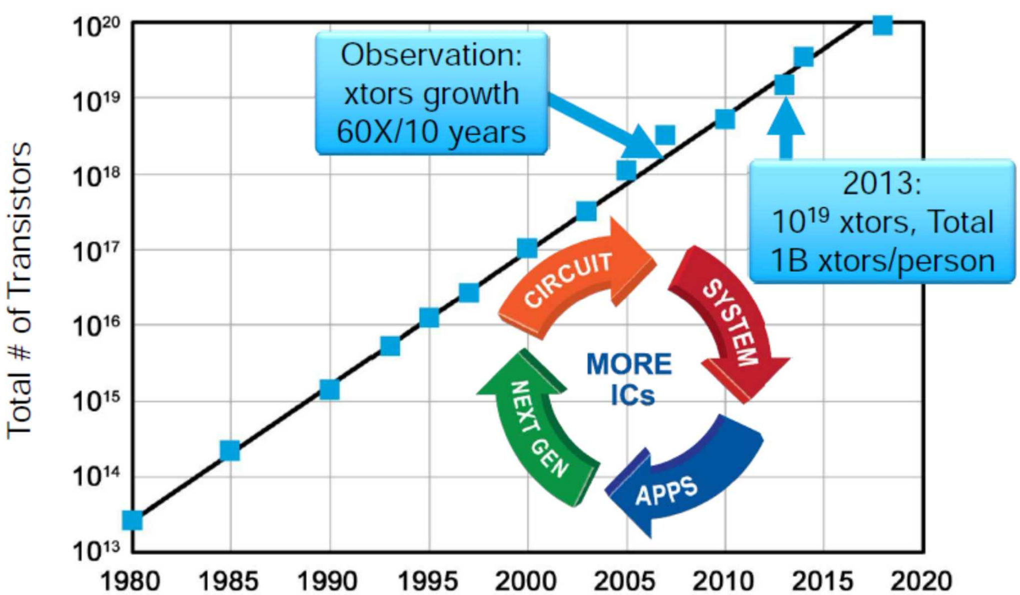
Steve Cowden
THE OREGONIAN
July 2007

Transistors Have Become Cheap



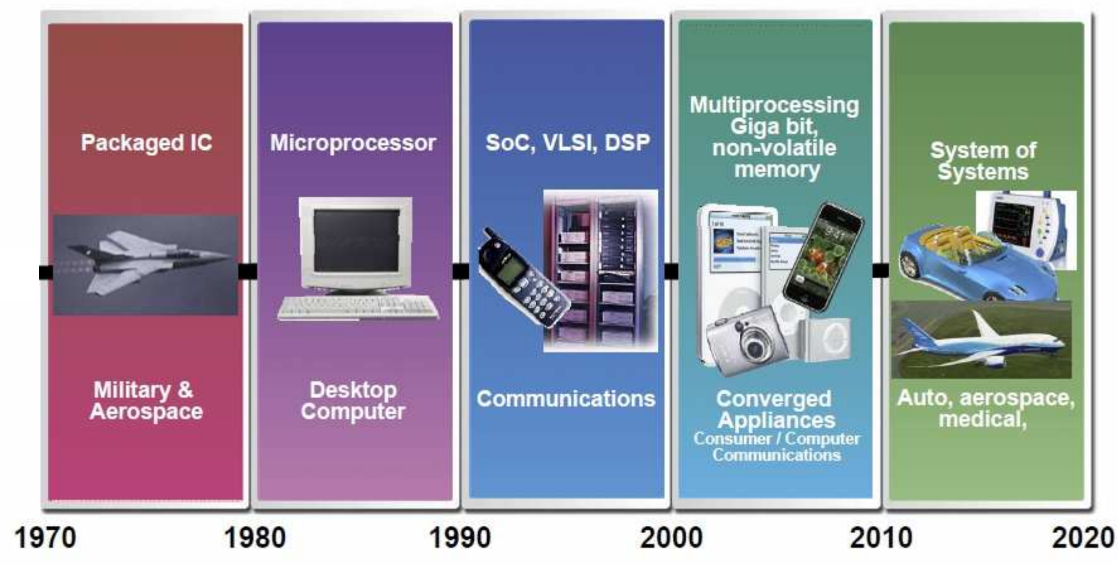
[Tsai, 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

Can Afford to Have Lots of Transistors



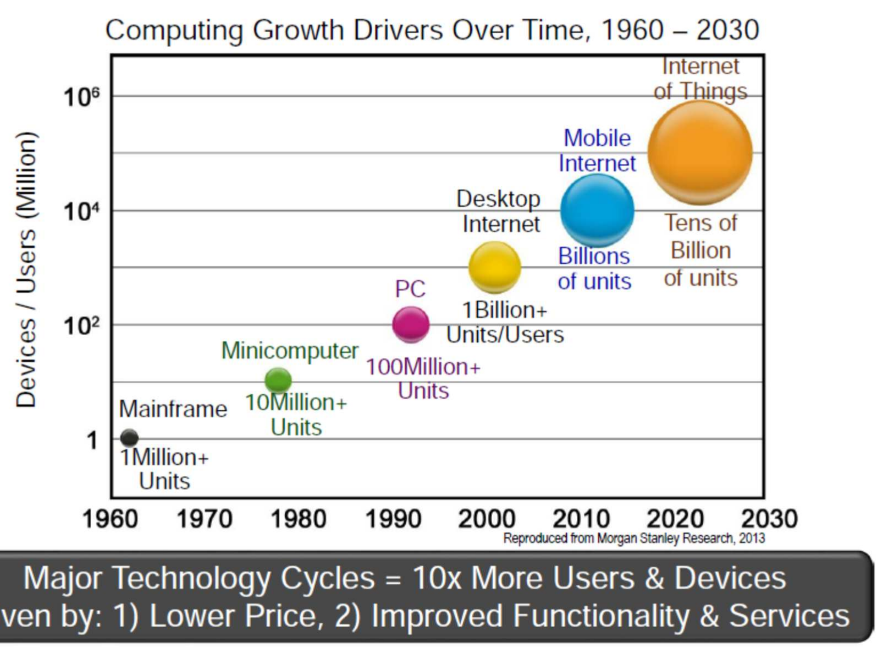
[Tsai, 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

Result: Increasingly Sophisticated Applications



[Walden Rhines, Mentor]

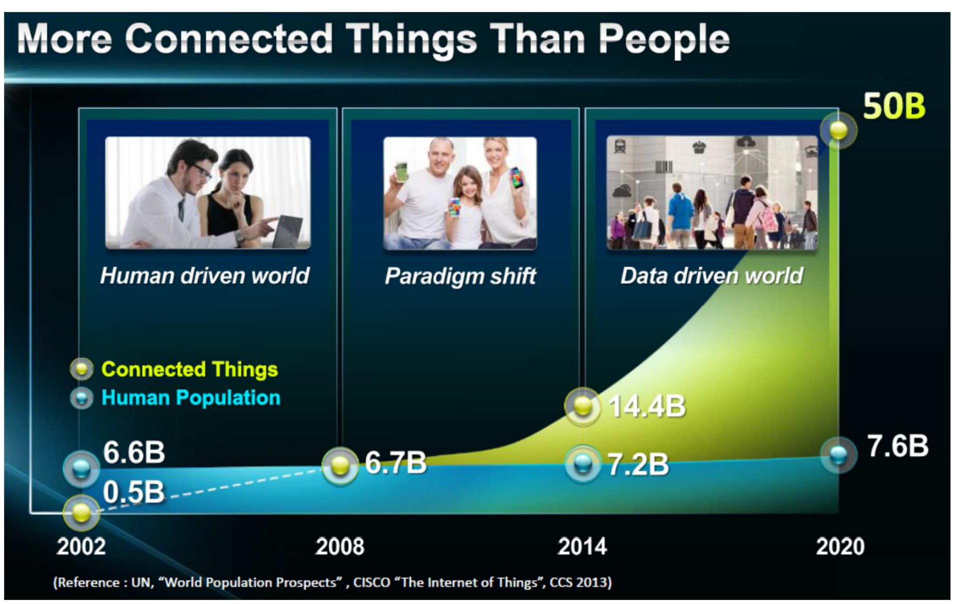
Drivers



[Tsai, 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

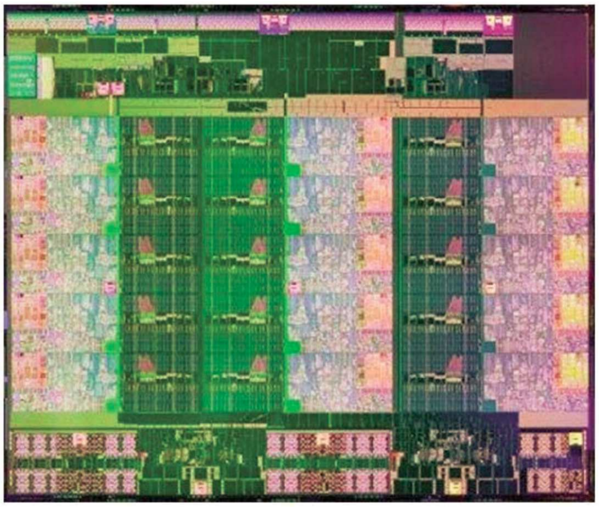
IoT Trend

[Tsai, 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]



[Kim, 2015 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

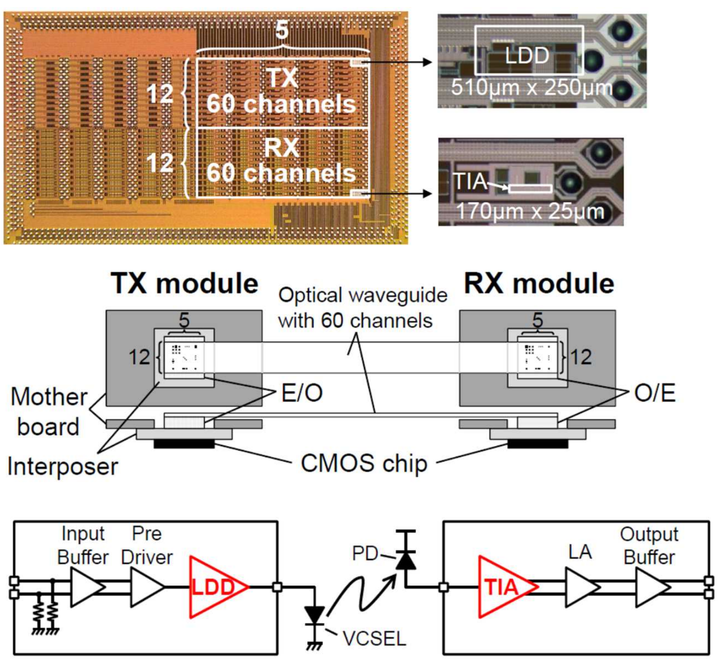
State-of-the-Art Microprocessor



Intel "Ivytown" Processor
15 Cores (64-bit)
22nm Technology
4.31 Billion Transistors
Clock Rate 1.4-3.8 GHz
Power Dissipation 40-150W

[Rusu, 2014 International Solid-State Circuits Conference (ISSCC)]

High-Speed Interconnect

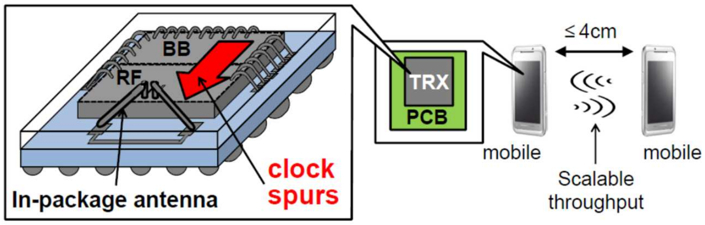


600 Gb/s optical chip-chip interface

Think about it:
600 Gb/s ~ 20 DVDs per second!

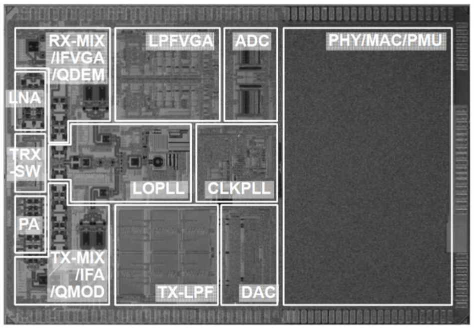
[Morita (Sony), 2014 International Solid-State Circuits Conference (ISSCC)]

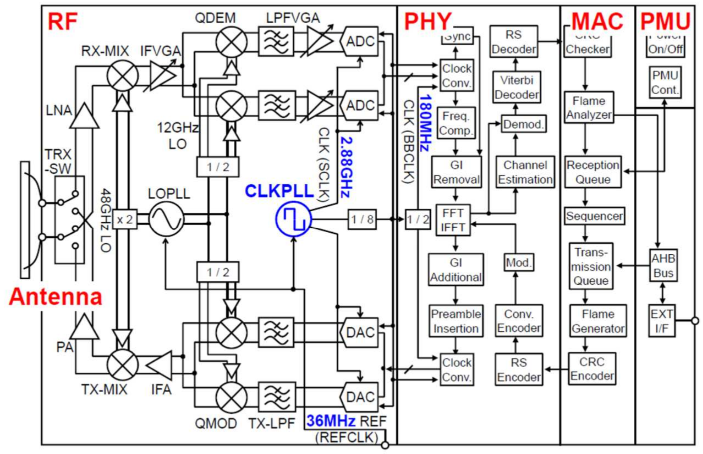
High Speed Wireless Interconnect



2 Gb/s link

60GHz CMOS Wireless Transceiver

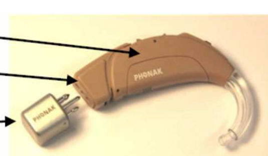


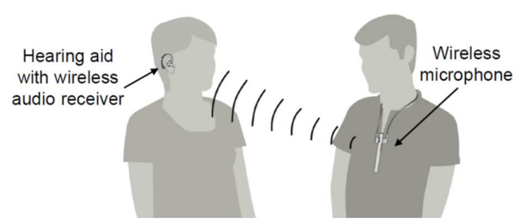


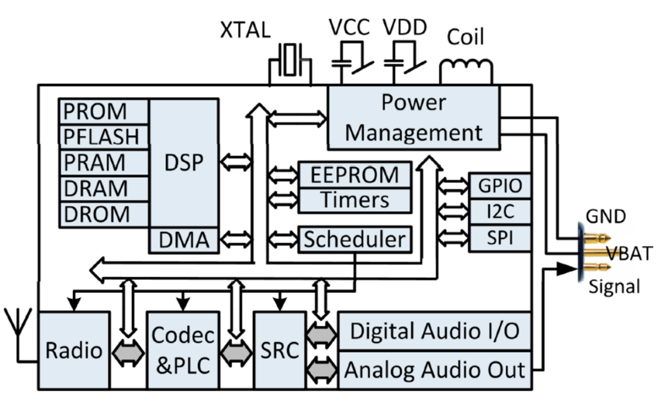
[Saigusa (Toshiba), 2014 International Solid-State Circuits Conference (ISSCC)]

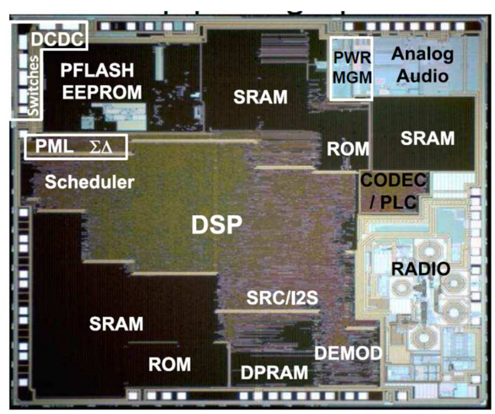
Hearing Aid with Wireless Receiver

Hearing aid
Audio “shoe” or “boot”
Wireless receiver



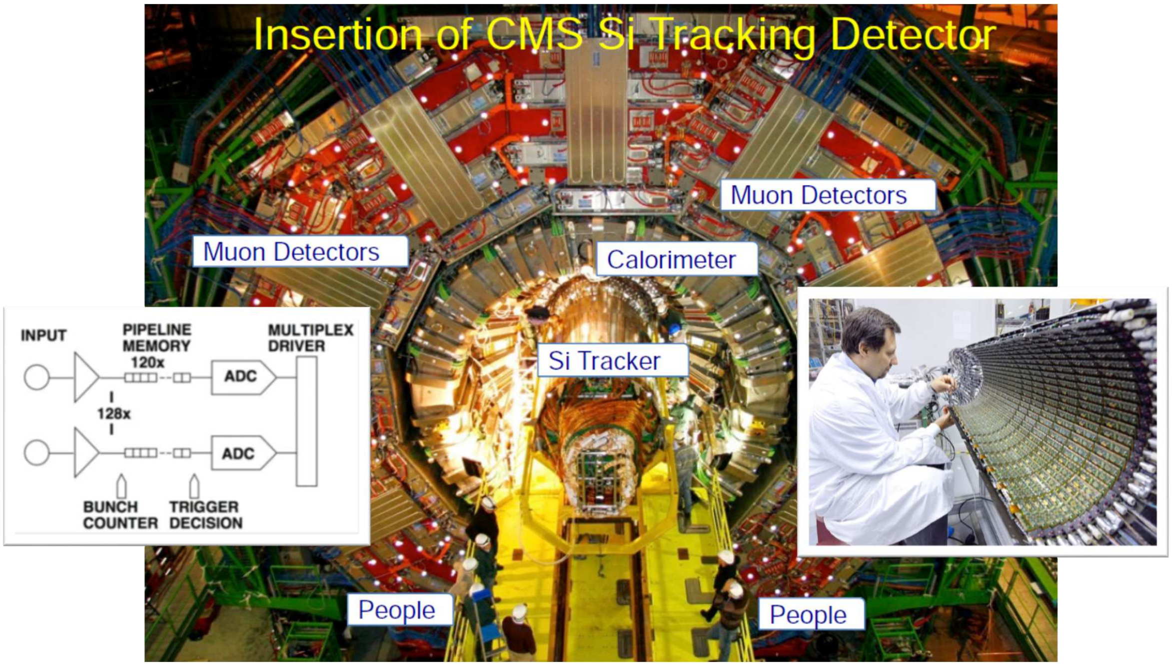




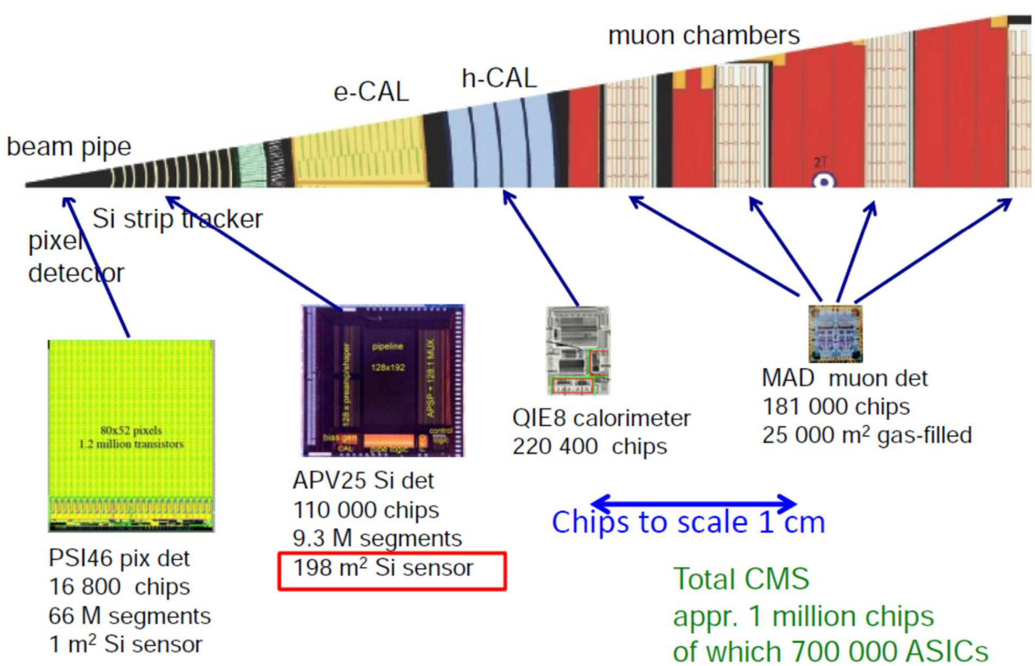


[El-Hoiydi, 2014 International Solid-State Circuits Conference (ISSCC)]

CERN CMS Experiment



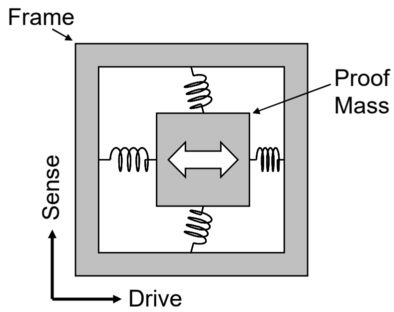
[Heijne (CERN), 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

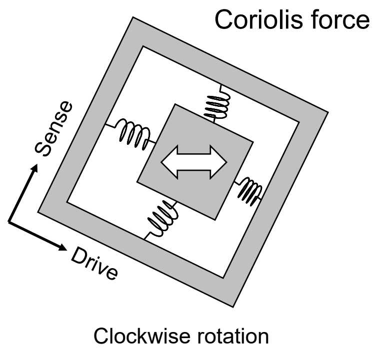


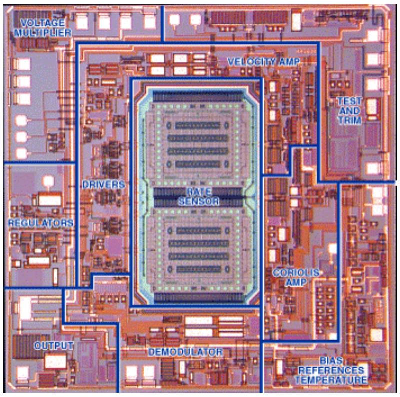
A huge sea of amplifiers and A/D converters!

[Heijne (CERN), 2014 International Solid-State Circuits Conference (ISSCC), Keynote Talk]

MEMS Gyroscope



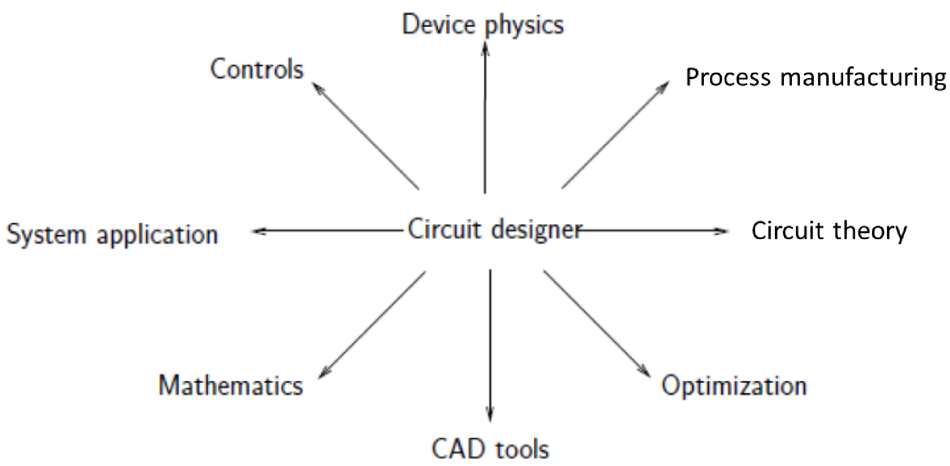




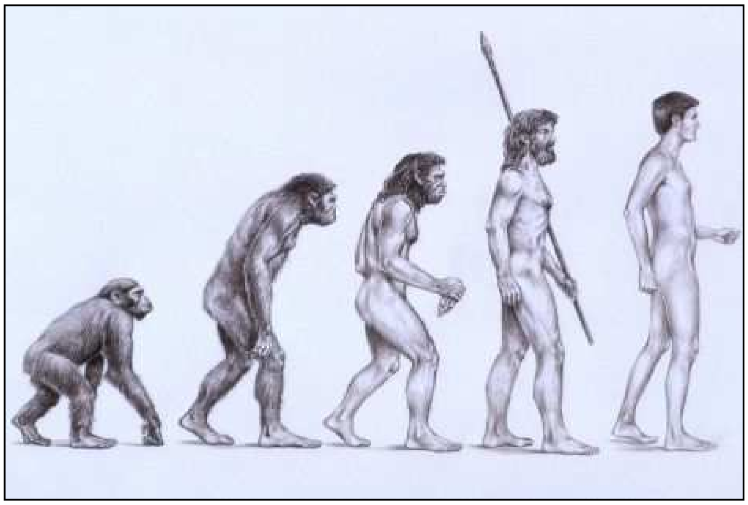
http://www.analog.com/library/analogDialogue/archives/37-03/gyro.html

- Proof mass oscillates ~10µm
- Rotation causes sub picometer displacement in sense direction
- Chip resolves a ΔC of 10^{-20} F in a BW of 1 Hz
- Corresponding displacement is 10^{-14} m, which is the classical radius of an electron (!)

Circuit Designers must be Broad!

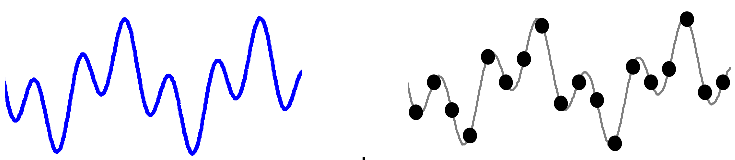


Learning All of This Takes Time!
The Evolution of a Circuit Designer



EE101A,B **EE114/214A** **EE214B** **EE314A,B**
EE315

Managing Complexity: Hierarchical Abstraction

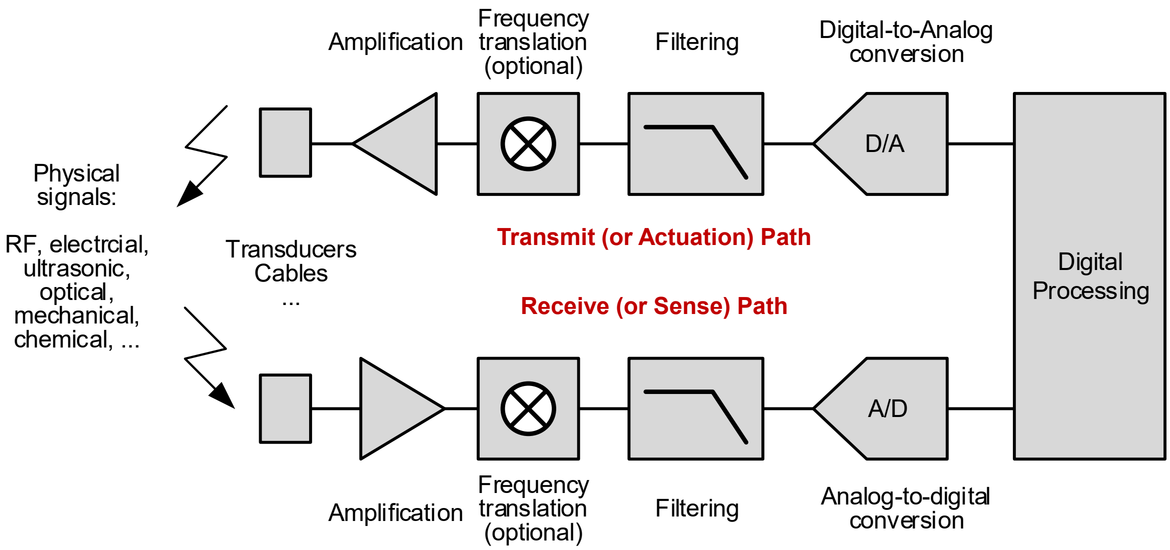


Analog | Digital

Mixed-Signal Systems	
Filters, Data Converters	Microprocessors
Operational Amplifiers	Arithmetic Blocks
Elementary Transistor Stages	Logic Gates
Device Modeling	
Device Physics	

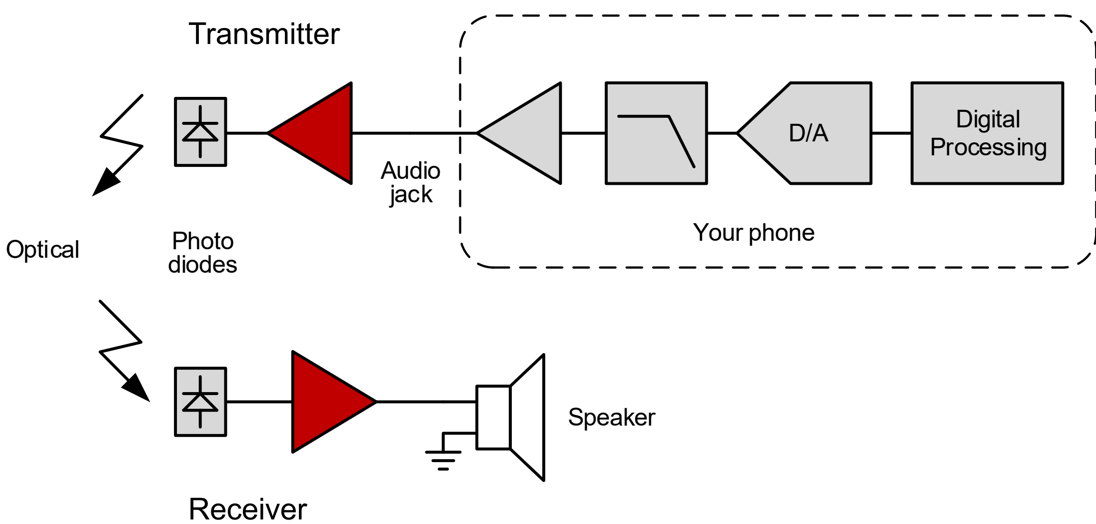
EE101B Playground

Managing Complexity: Block Abstraction



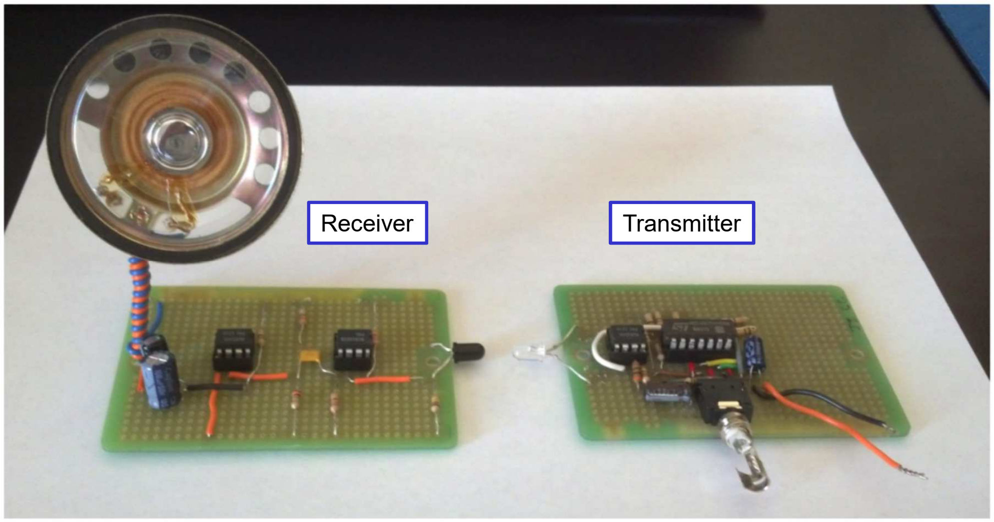
- Almost any meaningful electronic mixed-signal system can be represented by this generic block diagram

EE101B Lab



- Key aspect: "Signal conditioning" → manipulate the analog signal in such a way that it meets the requirements of the next stage or the connected transducer

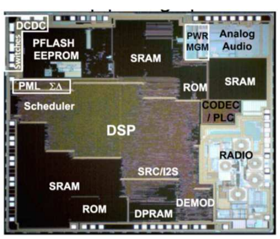
Final Lab Output

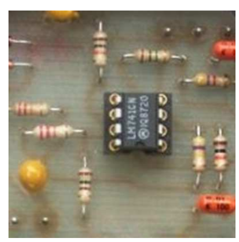


“Experience is what you get when you don’t get what you wanted.”

(Aaron Buchwald)

Integrated Circuit Design vs. Discrete Circuit Design





- Avoid using resistors and inductors, use as many MOSFET transistors as needed (within reasonable limits)
- Available capacitors are in the range of 10 fF–100 pF
- The critical parameters in transistors can be made to match to within 1%, but vary by more than 30% for different fabrication runs.
- Capacitors of similar size can match to within 0.1%, but vary by more than 10% for different fabrication runs.

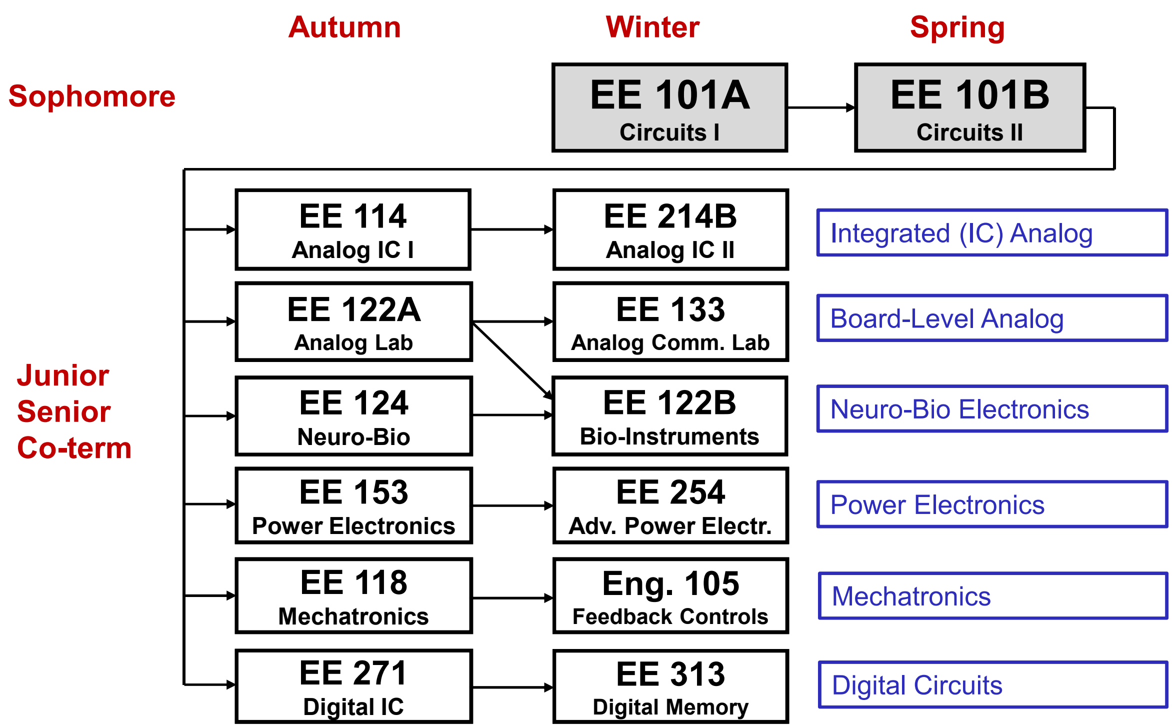
- Limit the component count below say 100 elements to achieve a small board area
- Available resistors can be chosen in the range of 1Ω–10 MΩ
- Available capacitors are in the range of 1 pF–10 mF
- All resistor are within 1–10% of their nominal values
- The utility of discrete transistors is limited. Use MOSFETs primarily as switches (power management). Usually prefer Opamps over discrete transistors. Sometimes use bipolar junction transistors if Opamps can’t do the job.

Apples vs. Oranges

Positioning of EE101B

- EE101B is **not** an IC design class
  - Continue with EE114 to learn circuit design techniques specific to integrated circuits
- EE101B is focused on the "common denominator" concepts for general circuit design
  - Most of the material forms the prerequisite for IC design but is also more broadly applicable

Many Possible Flows for Circuits-Oriented Students



Course Topics

- Modeling and analysis of analog gain stages
  - Two-port models
  - MOSFET operation
  - Biasing
  - Small-signal analysis
- Laplace transform for circuit designers
  - Frequency response
  - Step response
- Opamp-based feedback circuits
  - Stability and frequency compensation
  - Oscillators
  - Analog filters
- Circuit simulation
- Analog-to-digital conversion

Lab preparation

Textbook/Reference Material

- No required textbook!
- Use E40/EE101A-type textbooks when in doubt about fundamentals (on reserve in engineering library)
  - Ulaby and Maharbiz, "Circuits," 2nd ed.
  - Hambley, "Electrical Engineering: Principles and Applications," 6th ed.
  - Custom textbook from EE101A/Winter 2017
- Use EE114 textbook for introduction to gain stages
  - Murmann, "Analysis and Design of Elementary MOS Amplifier Stages"
  - Selected sections/chapters will be provided online
- Use various online resources and lecture notes for the more advanced topics

Prerequisites

- EE101A (required)
  - Kirchhoff's laws, superposition, Norton and Thevenin, PN junction, MOSFET I-V law, small-signal modeling, MOSFET single-stage amplifiers, energy storage elements
- EE102A (required)
  - LTI systems, sinusoids and complex exponentials, impulse response, convolution, frequency response, Fourier series, Fourier transform
- CME102 (recommended)
  - First- and second-order linear ODEs and their application to RLC circuits, transient and steady-state response, Laplace transform and its properties

Assignments

- Homework (20%)
  - Lowest homework score will be dropped
  - Handed out on Wednesdays, due following Wednesday at 5pm
  - We will collect the submitted homeworks from the gray collection box near Allen 208 at ~9am on Thursdays
- Lab (20%)
  - 8% pre-lab
  - 12% lab
- Midterm Exam (20%)
- Final Exam (40%)

Honor Code

- Please remember that you are bound by the honor code
  - We will trust you not to cheat
  - We will try not to tempt you
- But if you are found cheating it is very serious
  - There is a formal hearing
  - You can be thrown out of Stanford
- Save yourself a huge hassle and be honest
- For more info
  - http://www.stanford.edu/dept/vpsa/judicialaffairs/guiding/pdf/honorcode.pdf

Logistics

- Instructor
  - Boris Murmann, Allen 208
- Administrative Assistant
  - Ann Guerra, Allen 207
- Teaching assistants
  - TBD
- Web pages:
  - https://canvas.stanford.edu/courses/62873
    - Check regularly for office hours, etc.
  - https://piazza.com/stanford/spring2017/ee101b/home
    - For discussions
- This is a "paperless" course
  - All required materials provided on coursework page
- Discussion session
  - TBD

Lab Organization

- Lab meetings
  - Lab 1: Transistor characterization
  - Lab 2: Amplifier
  - Lab 3: Multistage amplifier
  - Lab 4: LED Driver
  - Lab 5: Opamp stability
  - Lab 6: Receiver & complete optical link
- Lab location
  - TBD
- You must sign up for a lab section during week 1, by Friday, April 7
  - Details to be announced

Chapter 2

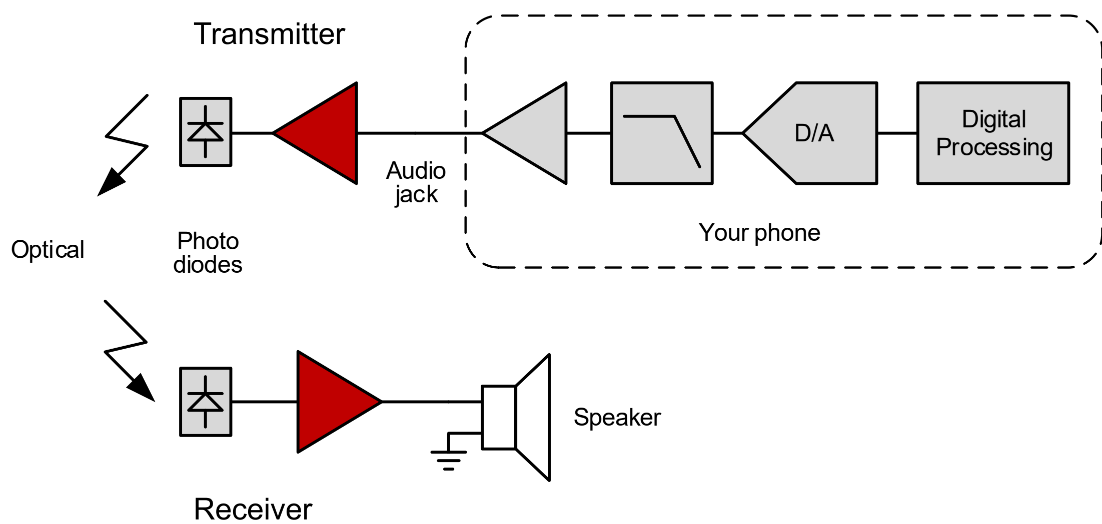
Two-Ports

Boris Murmann

Stanford University

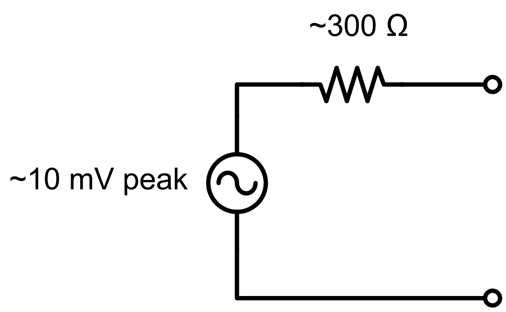
Reading: Murmann, Section 1-3

Motivation: EE101B Lab Project



- Key aspect: "Signal conditioning" → manipulate the analog signal in such a way that it meets the requirements of the next stage or the connected transducer

Model of Audio Jack



Transmit Photodiode

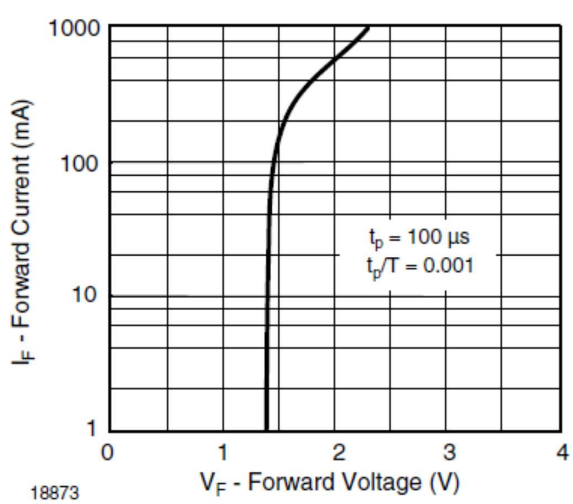
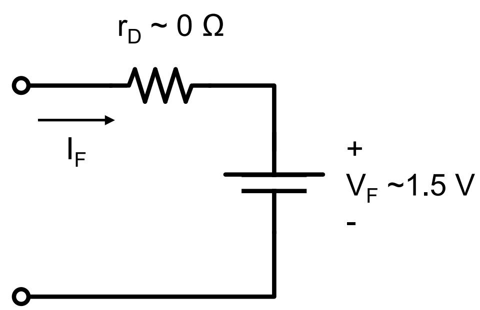


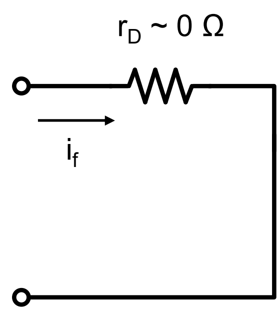
Fig. 4 - Forward Current vs. Forward Voltage

Model of Transmit Photodiode



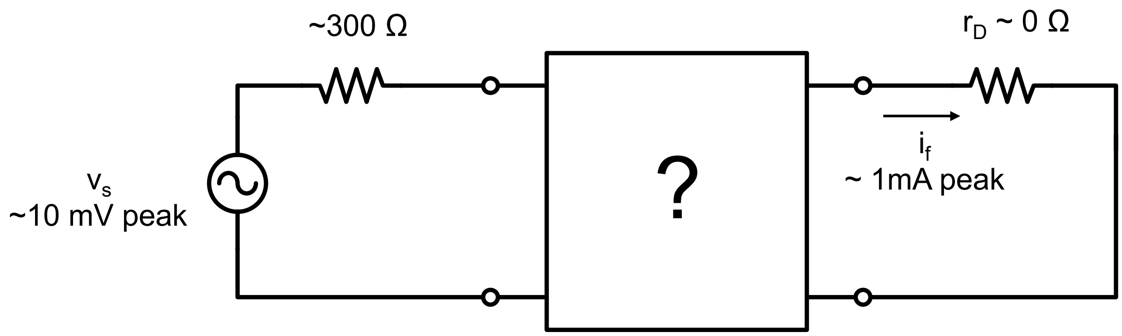
Emitted IR light proportional to I_F

Small-Signal Model of Transmit Photodiode



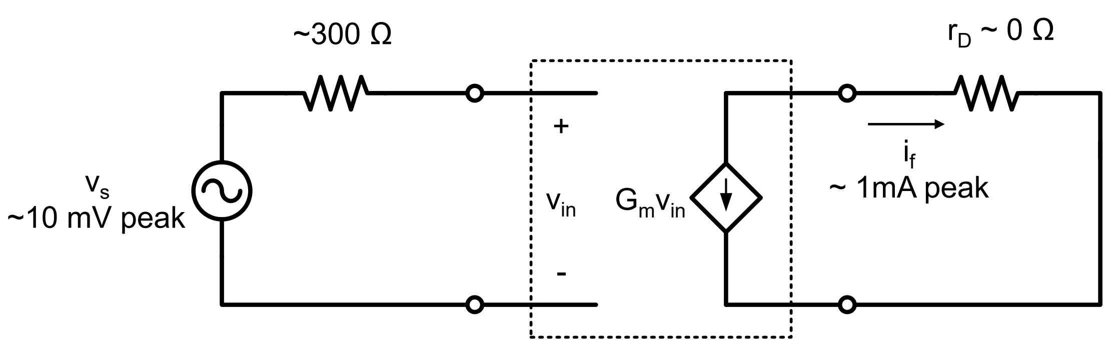
Want i_f ~1 mA peak for light modulation

How to Drive the Photodiode?



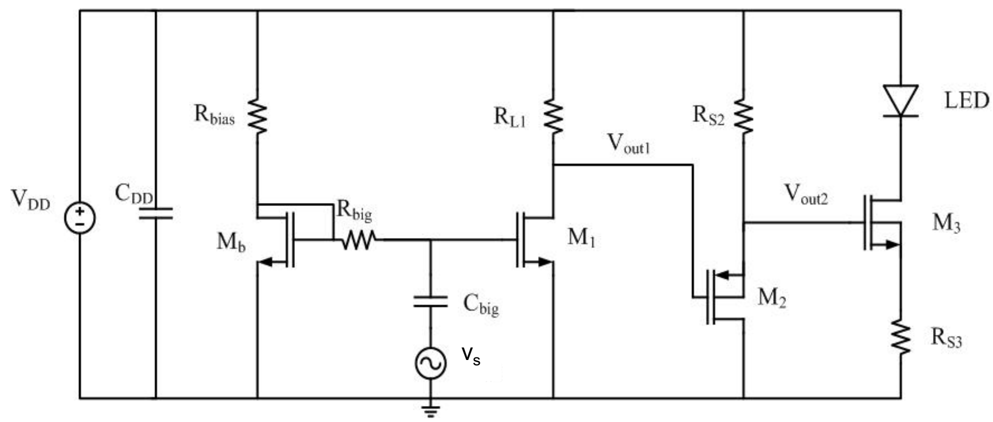
Solution

Transconductance amplifier



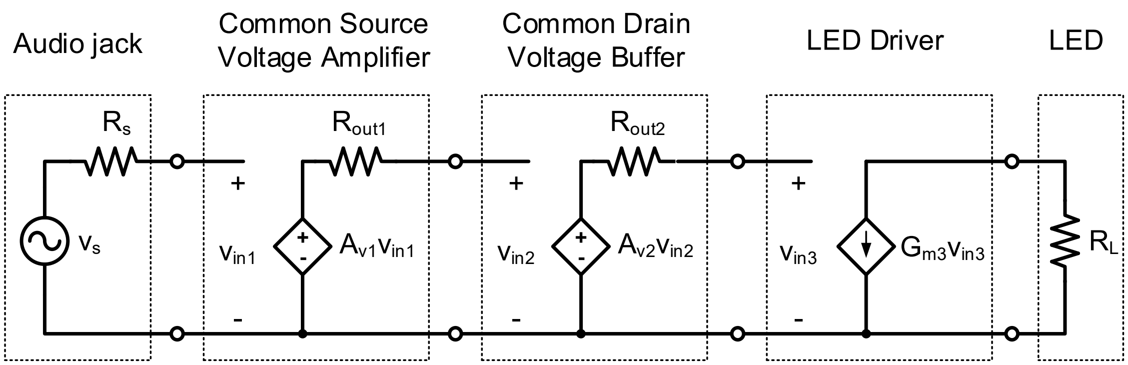
$$i_f = -G_m v_{in} = -G_m v_s \qquad G_m = -\frac{i_f}{v_s} = -\frac{1mA}{10mV} = -100mS$$

How We Will Realize This Circuit in The Lab



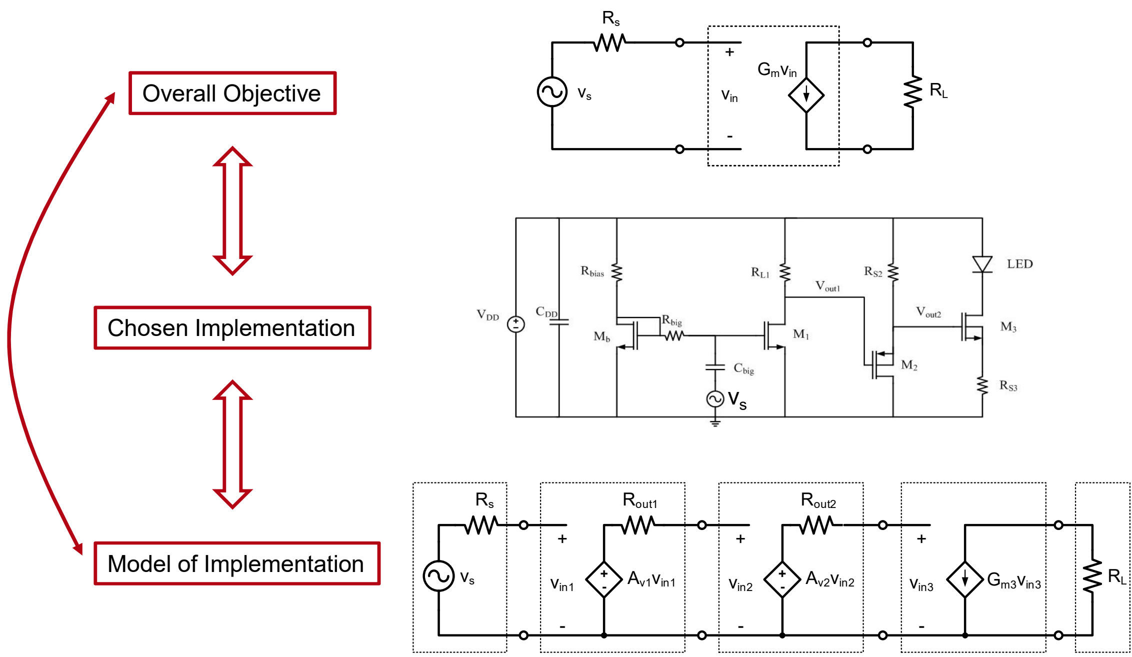
Biasing | Voltage Gain ~20 | Voltage Gain ~1 "Level Shift" | G_m ~ 5mS

Small-Signal Model of Lab Circuit



Voltage Amplifier | Voltage Amplifier | Transconductance Amplifier

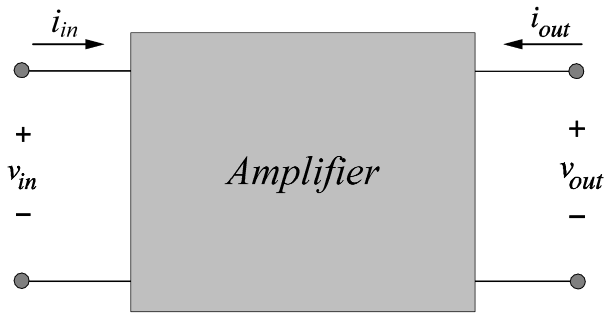
How a Circuit Designer Thinks About this Problem



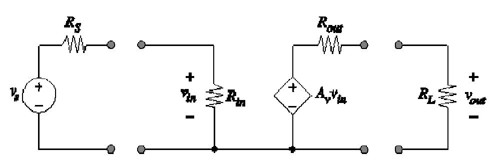
What we Need to Master

- Know the four types of two-port amplifiers
  - Voltage, current, transconductance, transresistance
- Know how to model arbitrary amplifier stages using two-port models
  - How to find the model parameters?
- Know how to work out cascade transfer functions
  - What is the overall transfer function of a chain of two-ports?

General Amplifier Two-Port

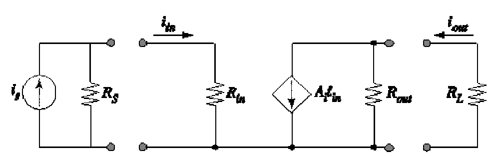


Currents defined to flow into the respective port
(somewhat arbitrary)



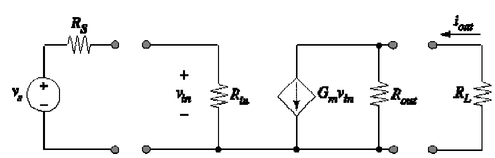
(a) VCVS

Voltage Amplifier Model



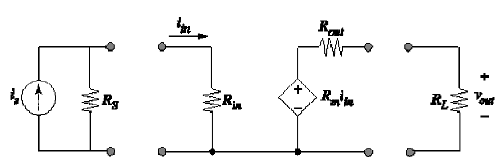
(b) CCCS

Current Amplifier Model



(c) VCCS

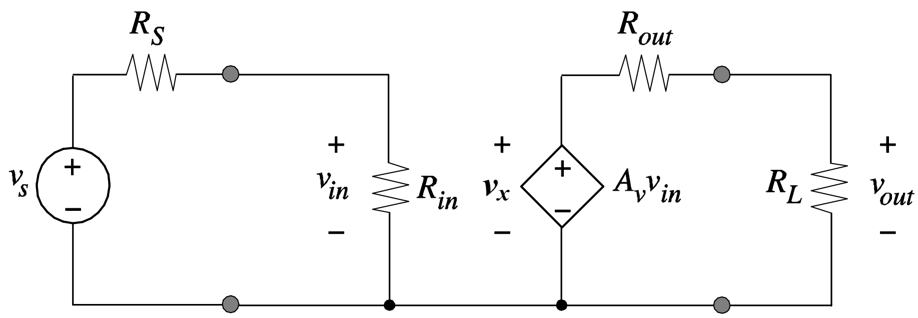
Transconductance Amplifier Model



(d) CCVS

Transresistance Amplifier Model

Overall Transfer Function of a Voltage Amplifier

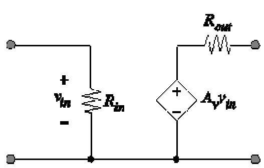


$$A_v' = \frac{v_{out}}{v_s} = \frac{v_{in}}{v_s} \cdot \frac{v_x}{v_{in}} \cdot \frac{v_{out}}{v_x}$$

$$A_v' = \frac{v_{out}}{v_s} = \frac{R_{in}}{R_{in} + R_s} \cdot A_v \cdot \frac{R_L}{R_L + R_{out}}$$

Why Not Model this as a Transconductance Amplifier?

- We can definitely do this!
- The two circuits below are equivalent
  - Thevenin → Norton

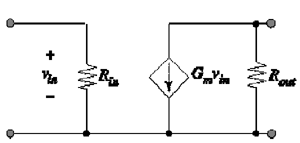


$$i_{sc} = \frac{A_v v_{in}}{R_{out}}$$

$$\frac{A_v v_{in}}{R_{out}} = -G_m v_{in}$$

$$\boxed{G_m = -\frac{A_v}{R_{out}}}$$

(for equivalency)



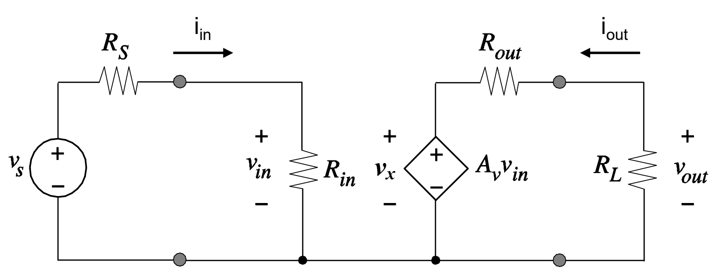
$$i_{sc} = -G_m v_{in}$$

- Furthermore, using appropriate Norton/Thevenin transformations at the input, we could just as well describe this circuit using a current amplifier or transresistance amplifier two-port
  – The four models can be parameterized to be exactly equivalent
- So then, why bother with four different models?
- The model we choose depends on the ***design intent***
  – Is the input signal represented by a current or a voltage?
  – Is the output signal represented by a current or a voltage?

Amplifier Type	**Input Quantity**	**Output Quantity**
Voltage Amplifier	Voltage	Voltage
Current Amplifier	Current	Current
Transconductance Amplifier	Voltage	Current
Transresistance Amplifier	Current	Voltage

How can We Tell?

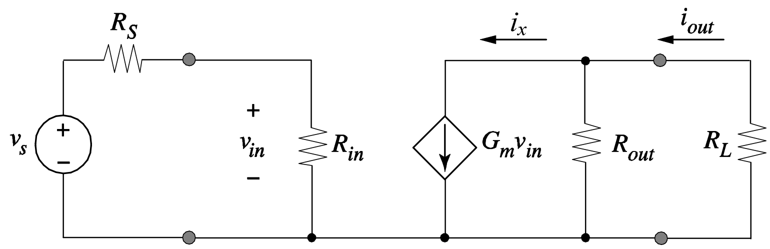
- Obviously, both the input and output port may carry both a voltage and current, so what do you mean?



If R_{in} << R_s, then the input voltage gets "destroyed" → the input is really the current
If R_L << R_{out}, then the output voltage gets "destroyed" → the output is really the current

$$A_v' = \frac{v_{out}}{v_s} = \frac{R_{in}}{R_{in} + R_s} \cdot A_v \cdot \frac{R_L}{R_L + R_{out}}$$

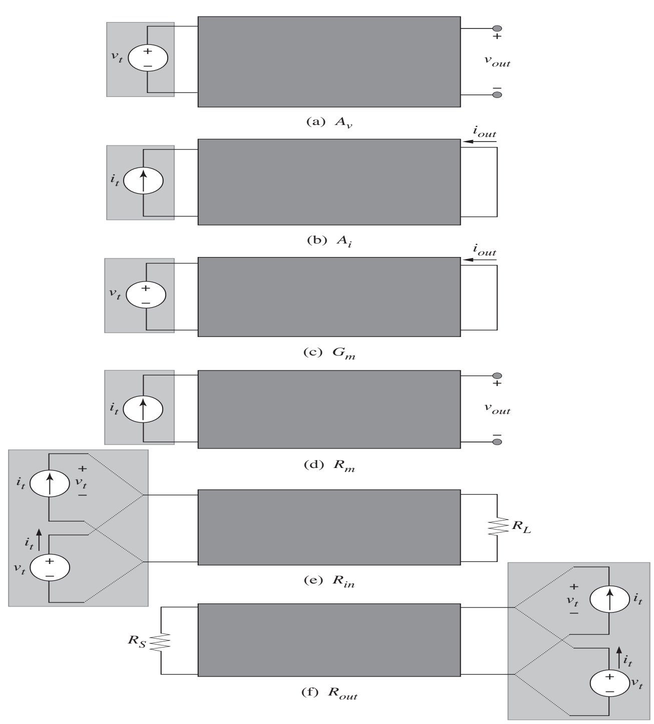
Another Example



$$G_m' = \frac{i_{out}}{v_s} = ?$$

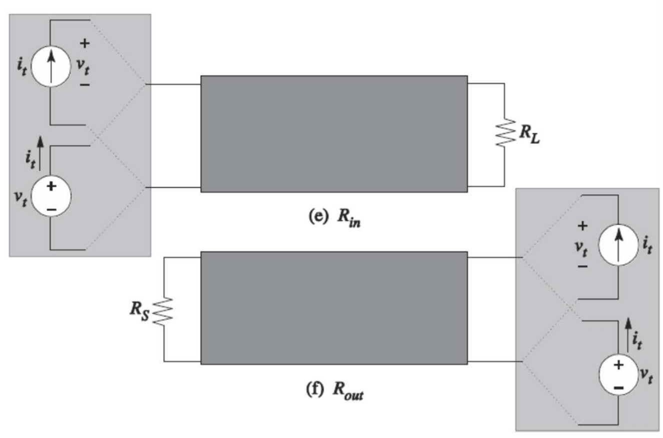
How to Calculate the Model Parameters of Arbitrary Circuits?

Step 1: Compute gain value



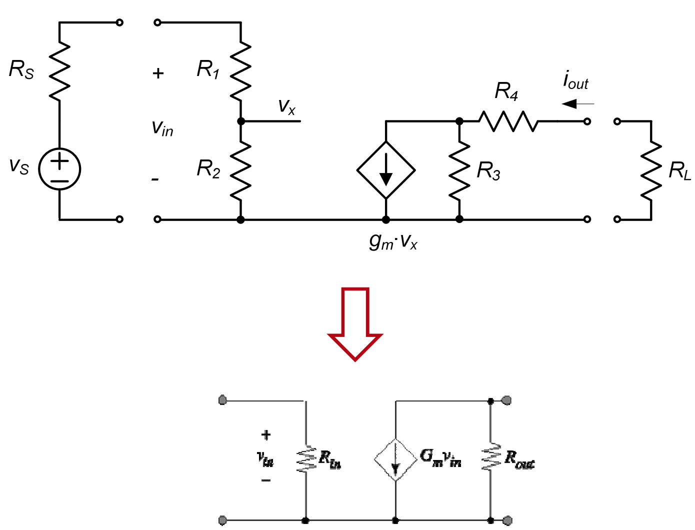
How to Calculate the Model Parameters of Arbitrary Circuits?

Step 2: Compute input and output resistances (or impedances)



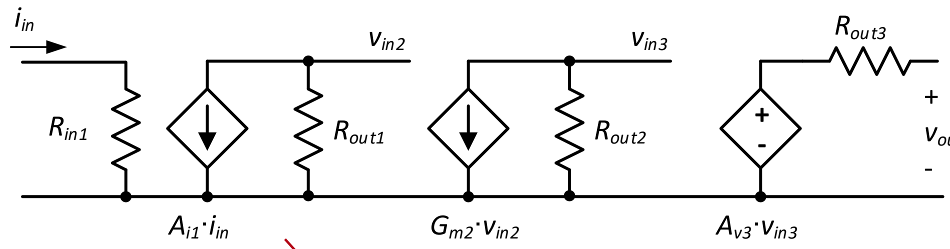
- R_L and R_S must be connected while applying the test source at the opposite port when the circuit is "bilateral" → beyond the scope of what we will discuss here (if you are interested, read Murmann, Example 1-3)

Example (Unilateral Circuit)



What are G_m, R_{in} and R_{out}?

Cascading Stages – A Simple Example



$$\frac{v_{out}}{i_{in}} = \frac{v_{in2}}{i_{in}} \cdot \frac{v_{in3}}{v_{in2}} \cdot \frac{v_{out}}{v_{in3}}$$

- Simply the product of individual transfer functions
- Solve using divide and conquer

What We Haven't Covered

- Intricacies of bilateral two-ports
  – We won't deal with these (much) in EE101B
- How to get to the small-signal model of a circuit
  – That's what we'll review next
- How to incorporate capacitors, inductors
  – We'll deal with this later in the quarter

Chapter 3

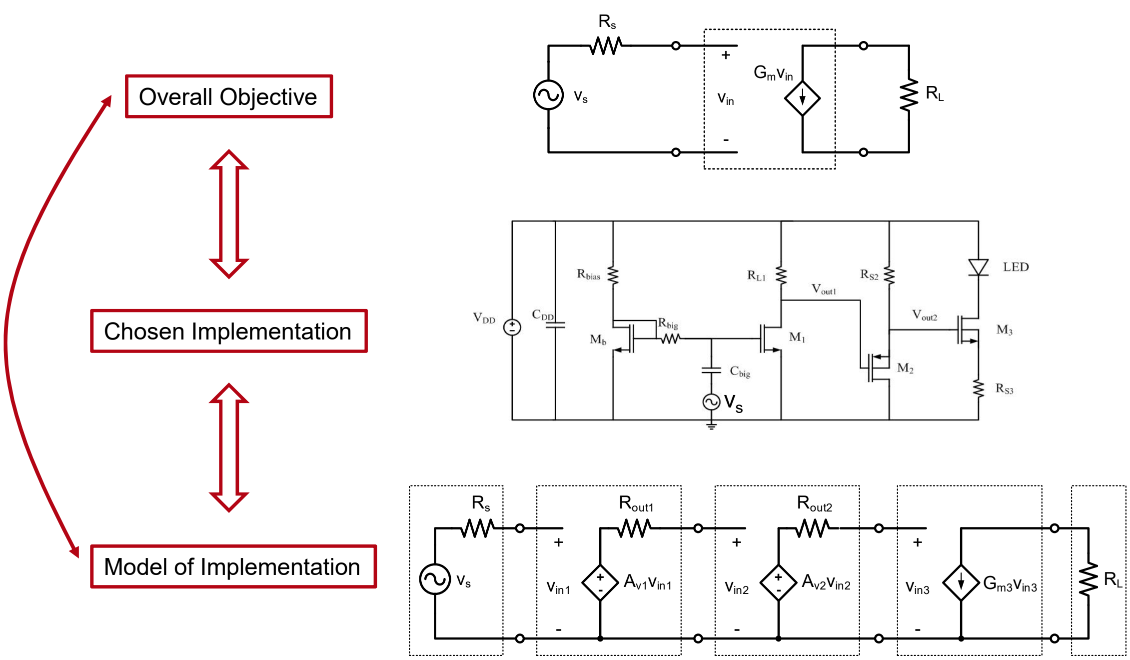
MOSFET Modeling

Boris Murmann

Stanford University

Reading: Murmann, Section 2-1

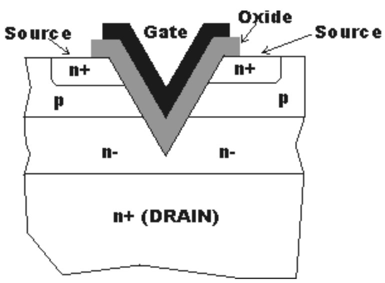
Motivation: Lab Transmitter Circuit

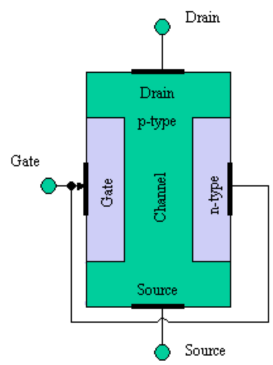


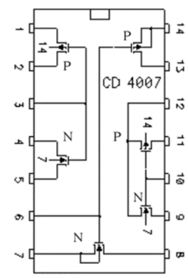
- How to model MOSFETs for our needs?

Field Effect Transistors Come in Many Shapes and Sizes

Power MOSFET

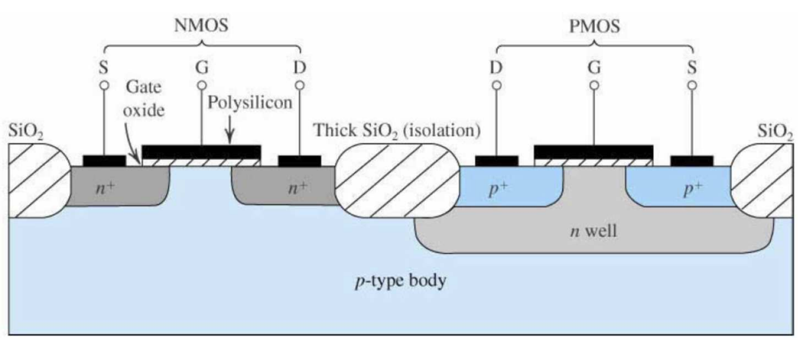






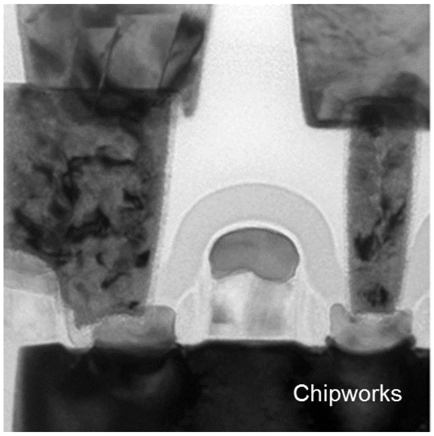
Field Effect Transistors Come in Many Shapes and Sizes

- In integrated circuits, the FETs are built as planar structures
- CMOS (Complementary Metal-Oxide-Semiconductor) technology features both n- and p-channel transistors

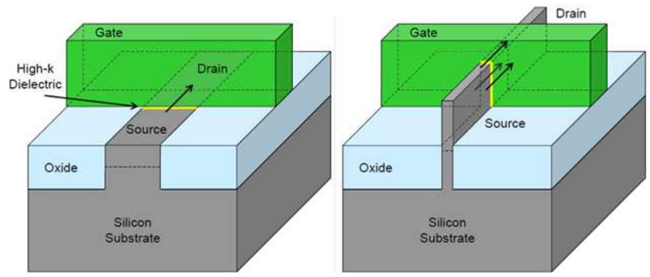


State of the Art

MOSFET with a gate length of 28nm



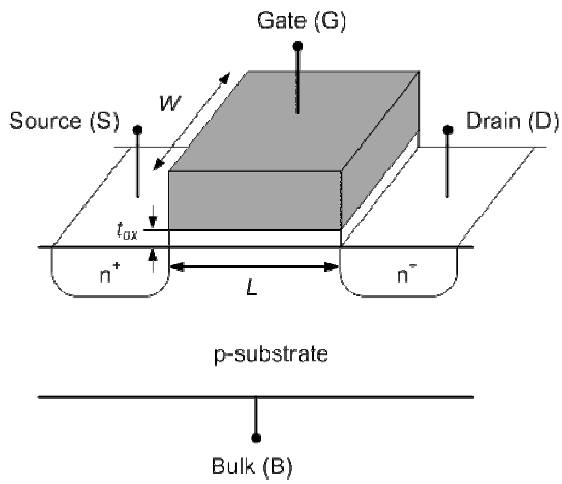
Current development: Shift from planar technology to 3D "FinFet" (or "TriGate") transistors

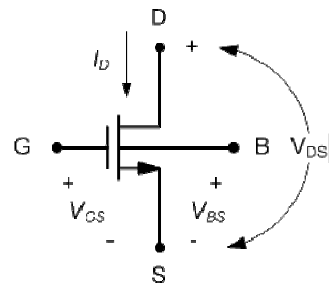


MOSFET Modeling in EE101B

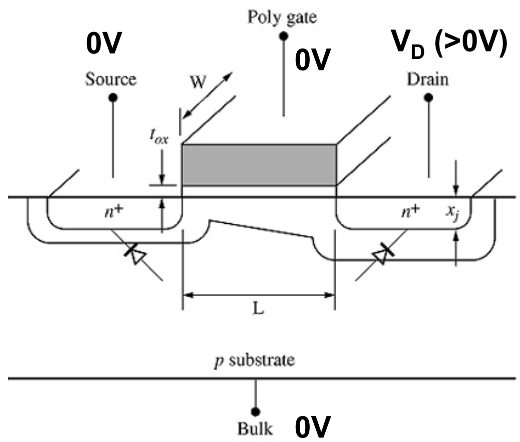
- Focus on the "bare minimum" fundamentals
- Will neglect many effects that can play a significant role in IC design
  - But have no bearing at all on the type of circuits we build in the lab
- Effects we will not take into account
  - Channel length modulation, backgate effect
    - See EE114
  - Drain induced barrier lowering, velocity saturation, mobility degradation, short channel effect, reverse short channel effect, subthreshold conduction, …
    - See EE216, EE214B

Structure of an Integrated (Planar) MOSFET



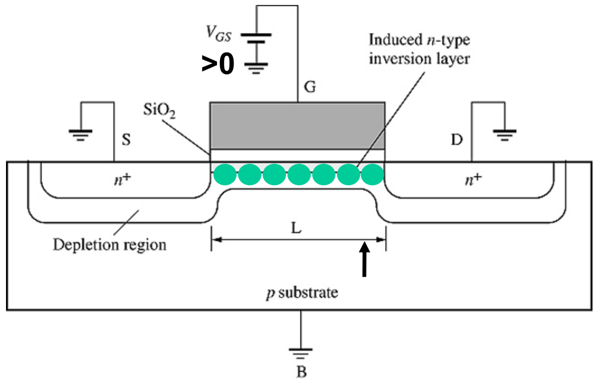


Basic MOS Operation (1)



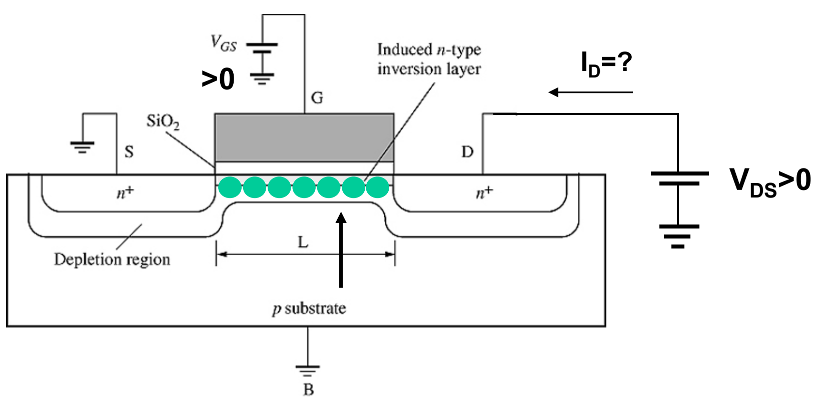
- With zero voltage at the gate, device is "off“
  - Back-to-back reverse biased pn junctions

Basic MOS Operation (2)



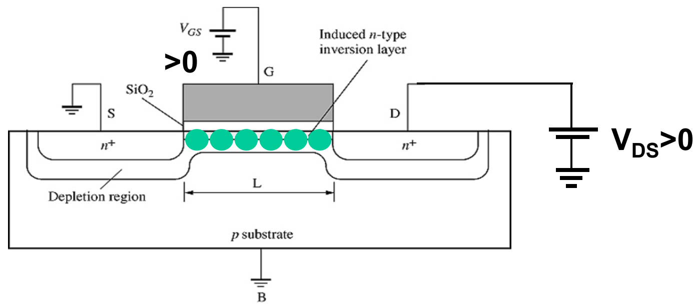
- With a positive gate bias applied, electrons are pulled toward the positive gate electrode
- Given a large enough bias, the electrons start to "invert" the surface ($p \rightarrow n$); a conductive channel forms
  - Threshold voltage, V_{Tn}

Basic Operation (3)



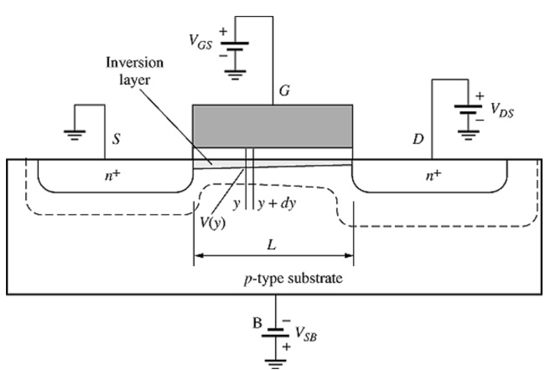
- If we now apply a positive drain voltage, current will flow
- How can we calculate this current as a function of V_{GS}, V_{DS}?

Assumptions



1) The current is controlled by the mobile charge in the channel
2) Gradual channel approximation - the vertical field sets channel charge, so we can approximate the mobile charge through the voltage difference between the gate and the channel
3) The carrier velocity is proportional to the lateral field ($\nu = \mu E$). This is equivalent to Ohm's law: velocity (current) is proportional to E-field (voltage)

First Order IV Characteristics (1)



- What we know:

$$Q_n(y) = C_{ox}\left[V_{GS} - V(y) - V_{Tn}\right]$$

$$I_D = Q_n \cdot v \cdot W$$

$$v = \mu_n \cdot E$$

$$\therefore I_D = C_{ox}\left[V_{GS} - V(y) - V_{Tn}\right] \cdot \mu_n \cdot E \cdot W$$

First Order IV Characteristics (2)

$$I_D = C_{ox}\left[V_{GS} - V(y) - V_{Tn}\right] \cdot \mu_n \cdot E \cdot W \qquad E = \frac{dV(y)}{dy}$$

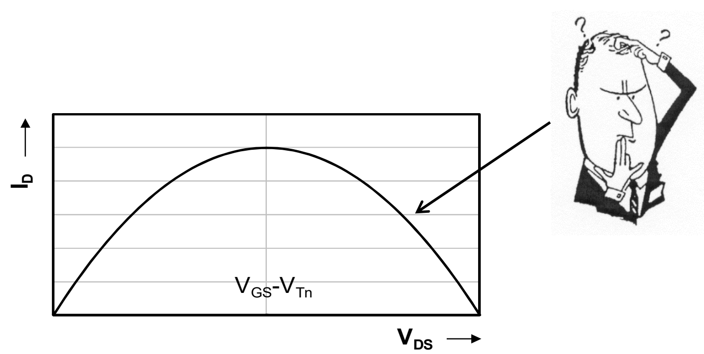
$$I_D dy = W\mu_n C_{ox}\left[V_{GS} - V(y) - V_{Tn}\right] \cdot dV$$

$$I_D \int_0^L dy = W\mu_n C_{ox} \int_0^{V_{DS}} \left[V_{GS} - V(y) - V_{Tn}\right] \cdot dV$$

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right) - \frac{V_{DS}}{2}\right] \cdot V_{DS}}$$

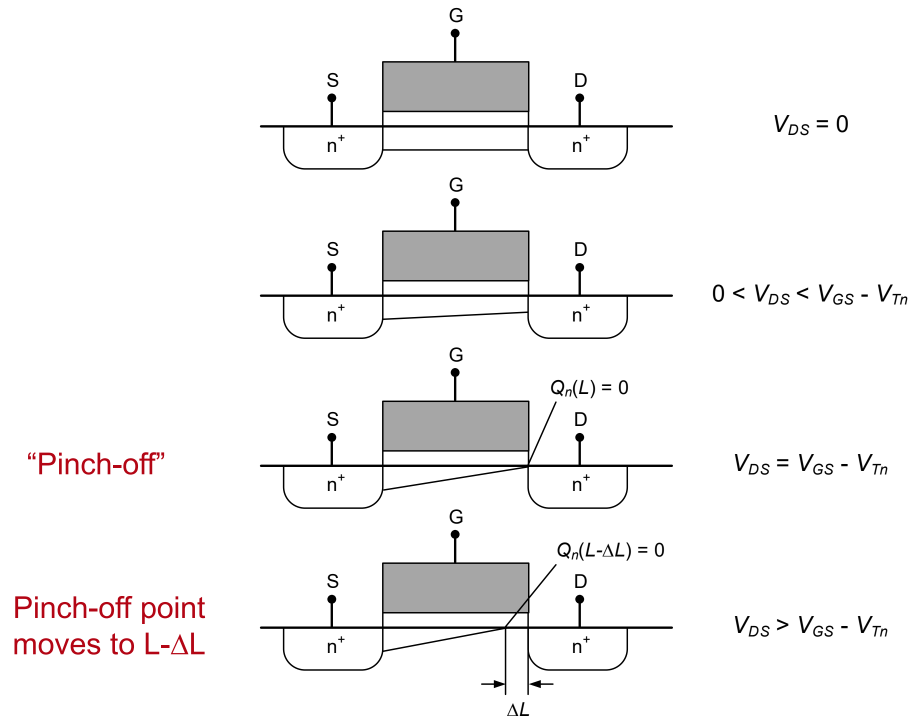
- For $V_{DS}/2 << V_{GS}-V_{Tn}$, this looks a lot like a linear resistor: $I=1/R \times V$
- Lets plot this IV relationship...

Plot of First Order IV Curves

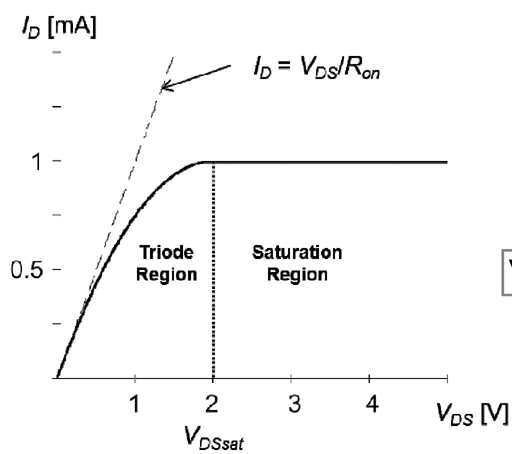


- Something is wrong here...
  - Current should never decrease with increasing V_{DS}
- What happens when $V_{DS}>V_{GS}-V_{Tn}$?
  - $V_{GD} = V_{GS}-V_{DS}$ becomes less than V_{Tn}, i.e. no more channel or "pinch off"

Progression of Channel Profile



Modified Plot and Equations



$$\boxed{V_{Dsat} = V_{GS} - V_{Tn}}$$

Triode:

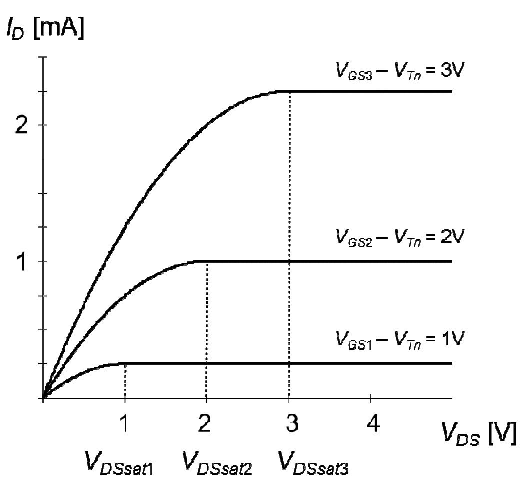
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right) - \frac{V_{DS}}{2}\right] \cdot V_{DS}$$

Saturation: (neglecting ΔL)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right) - \frac{(V_{GS} - V_{Tn})}{2}\right] \cdot (V_{GS} - V_{Tn}) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{Tn})^2$$

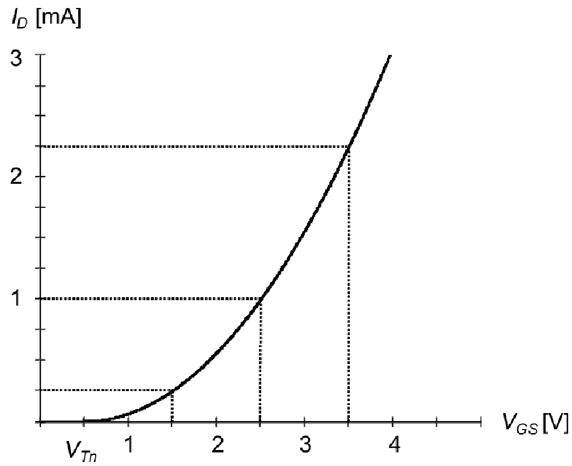
"Drain Characteristic"

Plot of I_D versus V_{DS} with V_{GS} as a parameter

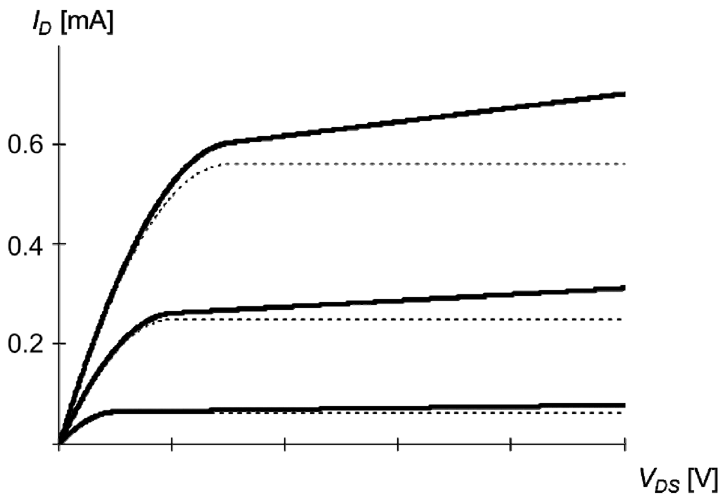


"Transfer Characteristic"

Plot of I_D versus V_{GS} in saturation (fixed V_{DS})



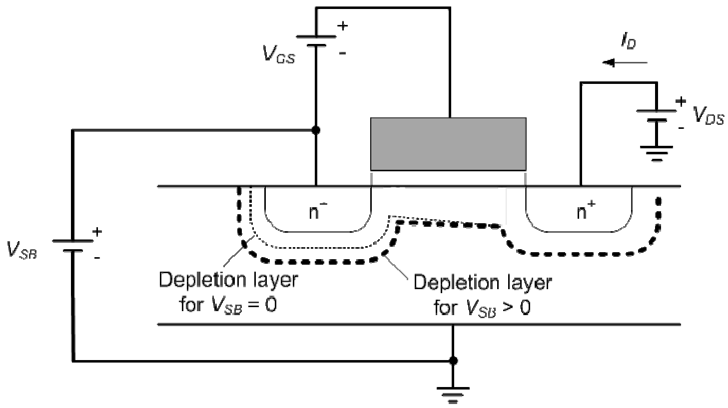
Channel Length Modulation ($\Delta L = f[V_{DS}]$)



In saturation: $$I_D \cong \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Tn})^2\left(\cancel{1+\lambda V_{DS}}\right)$$

We won't worry about this in EE101B

Backgate Effect

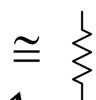


- If the bulk is not connected to the same potential as the source (as assumed previously), the threshold voltage becomes a function of VSB
- But, in EE101B, we will always connect the source to the bulk → $V_{SB} = 0$

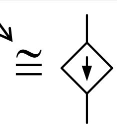
$$V_{Tn}(V_{SB}) = V_{TOn} + \cancel{\gamma_n}(\cancel{\sqrt{2\phi_f + V_{SB}}} - \cancel{\sqrt{2\phi_f}})$$

We won't worry about this in EE101B

First-Order MOS Model Summary



	"ON" $V_{GS} \geq V_{Tn}$	"OFF" $V_{GS} < V_{Tn}$
$V_{DS} < V_{DSsat}$	"Triode region" $I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right) V_{DS}$	$I_D = 0$
$V_{DS} \geq V_{DSsat}$	"Saturation region" $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn})^2$	



"VCCS" with quadratic control law

- For notational convenience, we define $V_{OV} = V_{GS} - V_{Tn}$
  - "Gate overdrive voltage"

EE101B Model Shortcomings to be Aware of

- We are neglecting channel length modulation, backgate effect
- For $V_{GS} < V_{Tn}$, the transistor is not 100% off, but carries a small current that scales exponentially with V_{GS}
- For short channels (say $L < 0.5\mu m$), various correction terms due to high electric fields must be included in the model
- For small values of V_{OV}, the physics are much more complicated than advertised. For the square law to hold, we require $V_{OV} > 150mV$.

- None of these issues will impair the kinds of circuits/experiments that we consider in EE101B
  - Take EE116, EE216, EE214B if you are interested…

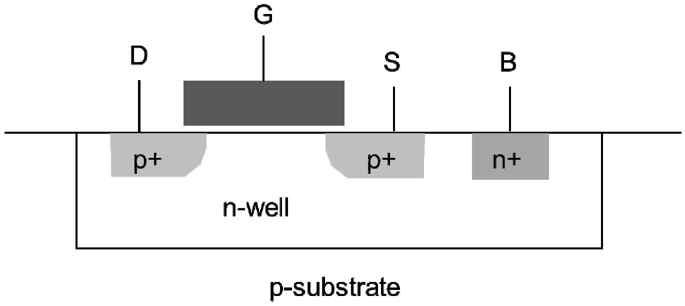
Which Parameters Can We Control?

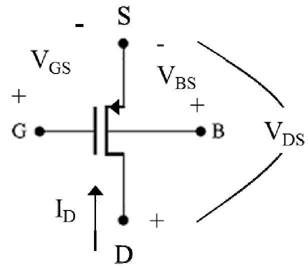
	IC Design (For a given, fixed fabrication process)	**Board level design** (For a given component, e.g. CD4007)
μ	No	No
C_{ox}	No	No
W, L	Yes	No
V_{Tn}	No (small changes possible via back-gate effect, or choice of L)	No (small changes possible via back-gate effect)

- Since we deal only with board level design in EE101B, it makes sense to lump together all the parameters that we cannot change, anyway. Define:

$$K = \mu C_{ox} \frac{W}{L}$$

P-Channel MOSFET





- I_D, V_{GS}, V_{DS}, and V_{Tp} are all negative → confusing algebra
- Solution: "**Think positive**," i.e. run right hand side of the IV equations will all positive numbers and know that the end result for I_D is negative

$$I_D = -K_p\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS}$$
$$I_D = -K_p\left[(-3V) - (-1V) - (-1V)\right](-1V)$$

⇨

$$-I_D = K_p\left(V_{SG} - \left|V_{Tp}\right| - \frac{V_{SD}}{2}\right)\cdot V_{SD}$$
$$-I_D = K_p\left[3V - 1V - 1V\right]\cdot 1V$$

Chapter 4

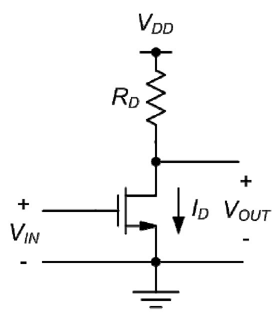
The Common-Source Stage

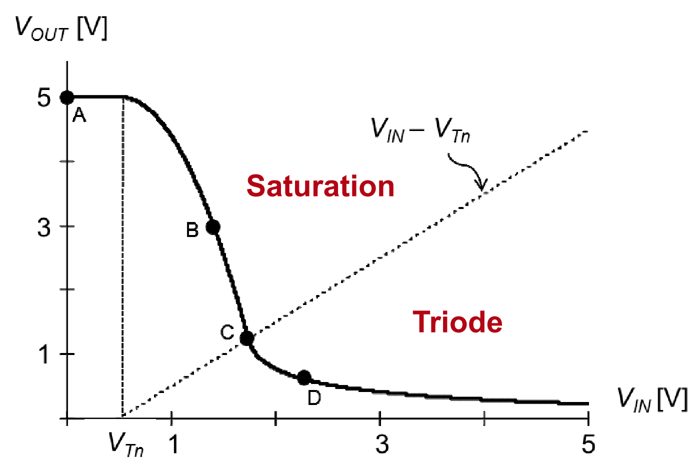
Boris Murmann

Stanford University

Reading: Murmann, Section 2-2; Pre-lab 2

Common-Source Stage

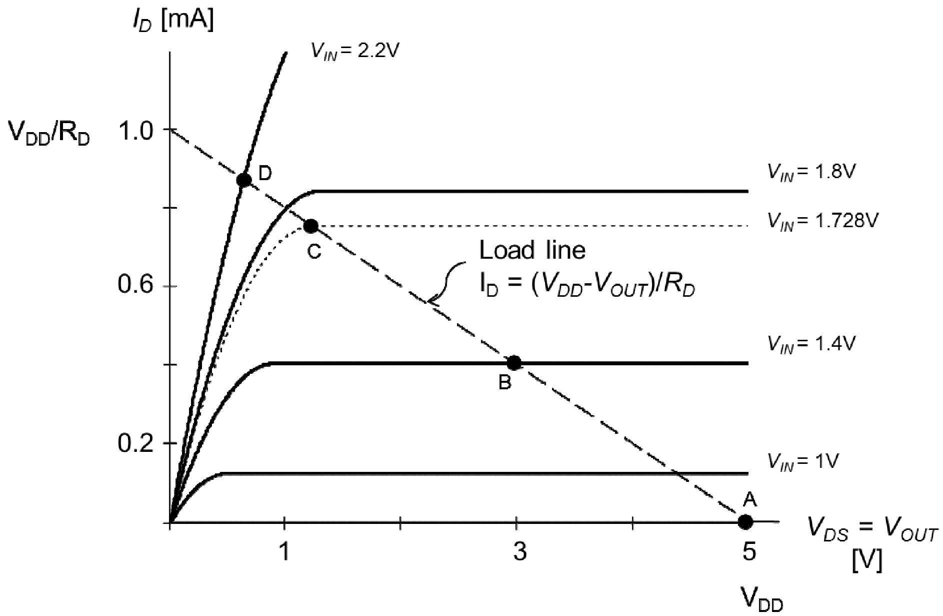




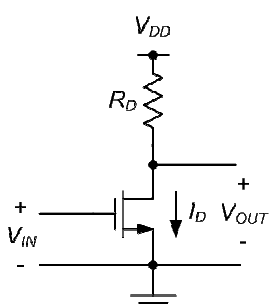
$$V_{OUT} = V_{DD} - I_D R_D$$

In saturation: $$V_{OUT} = V_{DD} - \frac{1}{2} K (V_{IN} - V_{Tn})^2 R_D$$

Load Line Perspective



Example



$$V_{DD} = 5\ V$$

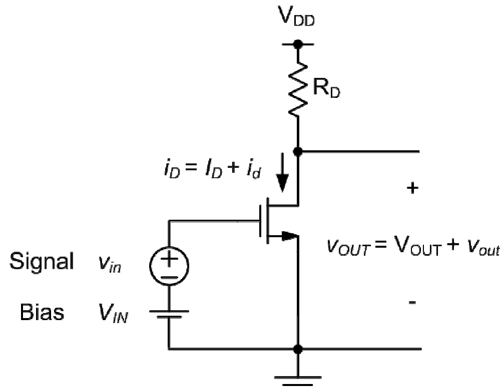
$$R_D = 10\ k\Omega$$

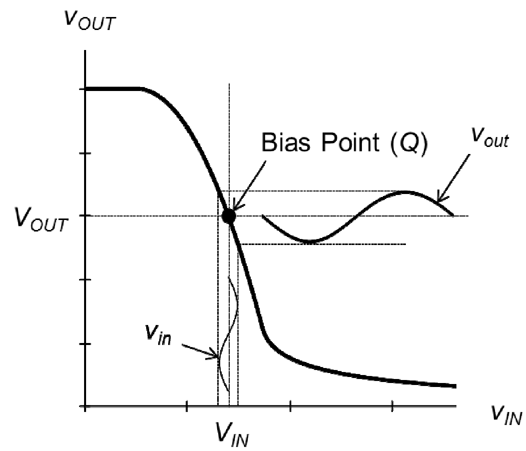
$$K = 500\ \frac{\mu A}{V^2}, V_{Tn} = 1.5V$$

$$Want\ \ V_{OUT} = 2.5\ V$$

- What is the required V_{IN}?
- Does the transistor operate in saturation or in the triode region?

Biasing and Small-Signal Analysis





- The input is decomposed into a DC bias component (V_{IN}) and a small-signal AC component (v_{in}); same for drain current and output voltage

$$v_{IN} = V_{IN} + v_{in} \qquad i_D = I_D + i_d \qquad v_{OUT} = V_{OUT} + v_{out}$$

$$V_{OUT} = V_{DD} - \frac{1}{2}K(V_{IN} - V_{Tn})^2 R_D$$

This equation must hold for the DC quantities (in saturation)

$$v_{OUT} = V_{DD} - \frac{1}{2}K(v_{IN} - V_{Tn})^2 R_D$$

It must also hold for the total quantities

$$V_{OUT} + \boldsymbol{v_{out}} = V_{DD} - \frac{1}{2}K(V_{IN} + v_{in} - V_{Tn})^2 R_D$$

What we want to know

$$v_{out} = \cancel{V_{DD}} - \frac{1}{2}K(V_{IN} + v_{in} - V_{Tn})^2 R_D - \cancel{V_{DD}} + \frac{1}{2}K(V_{IN} - V_{Tn})^2 R_D$$

$$(a+b)^2 - a^2 = 2ab + b^2 \qquad a = V_{IN} - V_{Tn} \qquad b = v_{in}$$

$$v_{out} = -\frac{1}{2}KR_D\left[2(V_{IN} - V_{Tn})v_{in} + v_{in}^2\right]$$

$$v_{out} = -KR_D(V_{IN} - V_{Tn})v_{in}\left[1 + \frac{v_{in}}{2(V_{IN} - V_{Tn})}\right]$$

$$v_{out} = -KR_D V_{OV} v_{in}\left[1 + \cancel{\frac{v_{in}}{2V_{OV}}}\right]$$

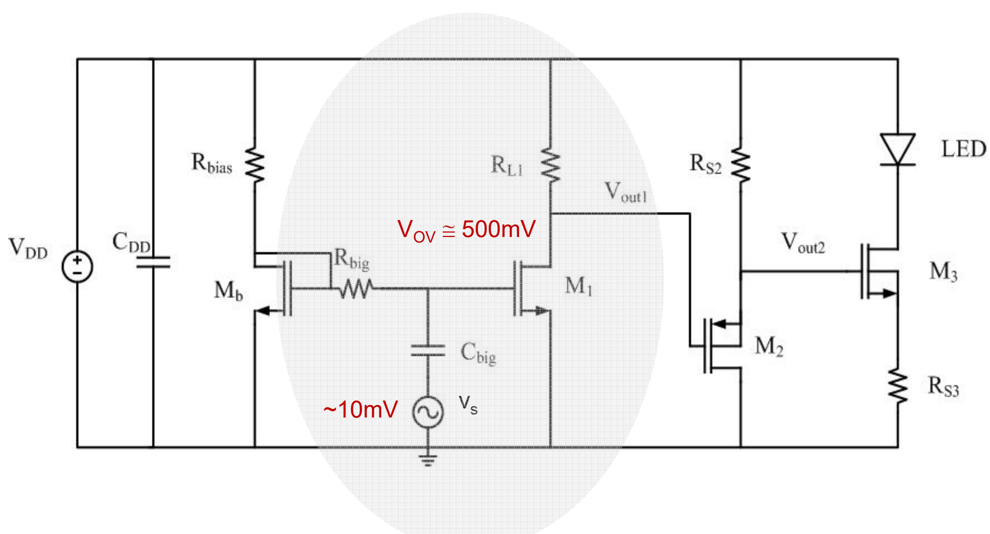
Small-signal approximation: $v_{in} \ll 2V_{OV}$

Linear amplifier model:

$$A_v = \frac{v_{out}}{v_{in}} = -KV_{OV}R_D$$

Valid if: (1) device operates in saturation, (2) $v_{in} << 2V_{OV}$

Lab Transmitter Circuit



→ The small signal approximation is valid for the CS stage realized by M1

Alternative Approach

Taylor expansion of a differentiable function around point *a*:

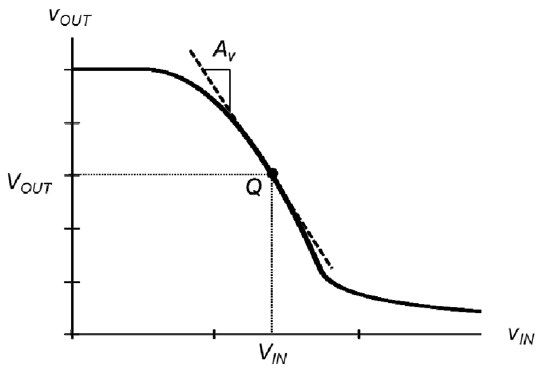
$$f(x) = f(a) + \frac{f'(a)}{1!}(x-a) + \cancel{\frac{f''(a)}{2!}(x-a)^2} + \cdots$$

For our circuit:

$$v_{OUT} = V_{OUT} + \left.\frac{dv_{OUT}}{v_{IN}}\right|_{v_{IN}=V_{IN}} (v_{IN} - V_{IN})$$

$$v_{OUT} - V_{OUT} = \left.\frac{dv_{OUT}}{v_{IN}}\right|_{v_{IN}=V_{IN}} (v_{IN} - V_{IN})$$

$$v_{out} = \left.\frac{dv_{OUT}}{v_{IN}}\right|_{v_{IN}=V_{IN}} v_{in}$$



$$\boxed{A_v = \frac{v_{out}}{v_{in}} = \left.\frac{dv_{OUT}}{v_{IN}}\right|_{v_{IN}=V_{IN}}}$$

$$A_v = \frac{v_{out}}{v_{in}} = \left.\frac{dv_{OUT}}{v_{IN}}\right|_{v_{IN}=V_{IN}} = \frac{d}{dv_{IN}}\left[V_{DD} - \frac{1}{2}K(v_{IN} - V_{Tn})^2 R_D\right]_{v_{IN}=V_{IN}}$$

$$A_v = \frac{v_{out}}{v_{in}} = [-K(v_{IN} - V_{Tn})R_D]_{v_{IN}=V_{IN}}$$

$$A_v = \frac{v_{out}}{v_{in}} = -K(V_{IN} - V_{Tn})R_D = -KV_{OV}R_D$$

- Exactly the same result as before
- However, the issue with both approaches we've used so far is that we first have to write out the large signal transfer function
  - This can get tedious for larger circuits
- Much more elegant: Instead of differentiating the large signal transfer function, **"differentiate" (linearize) each component in the circuit**

Why Should This Work?

- No matter how nonlinear or complex a circuit is, it has to obey KCL and KVL. For each node, all of the DC bias currents and all incremental currents have to sum to zero:

$$0 = I_1 + I_2 + I_3 + \cdots \qquad\qquad 0 = i_1 + i_2 + i_3 + \cdots$$

- In general, the incremental currents can be arbitrary (nonlinear) functions of the incremental node voltages (around the operating point)

$$i_j = f_j(v_1, v_2, v_3, \dots)$$

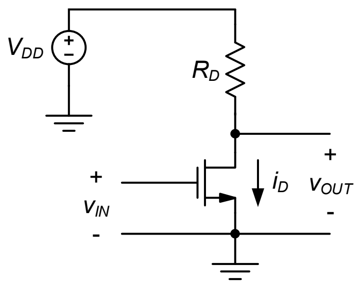
- If all excursions are small, we can approximate them via the total differential, where all derivatives are evaluated at the operating point (Q) and KCL will still hold in the limit sense

$$di_j = \left.\frac{\partial f_j}{\partial v_1}\right|_Q dv_1 + \left.\frac{\partial f_j}{\partial v_2}\right|_Q dv_2 + \left.\frac{\partial f_j}{\partial v_3}\right|_Q dv_3 + \cdots \qquad \sum di_j \cong \sum i_j = 0$$

- We can argue exactly the same way for KCL and express small voltage excursions around the operating point via a total differential

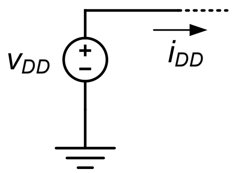
$$dv_j = \left.\frac{\partial g_j}{\partial i_1}\right|_Q di_1 + \left.\frac{\partial g_j}{\partial i_2}\right|_Q di_2 + \left.\frac{\partial g_j}{\partial i_3}\right|_Q di_3 + \cdots \qquad \sum dv_j \cong \sum v_j = 0$$

- The bottom line is that we can differentiate all i-v and v-i relationships to predict the circuit behavior for small excursions around the operating point
- No worries – this will be much easier than it looks, since f() and g() are typically just one dimensional or two-dimensional functions
  - We just wrote the full-blown equations above to get a feel for why the approach must work in general

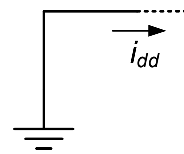


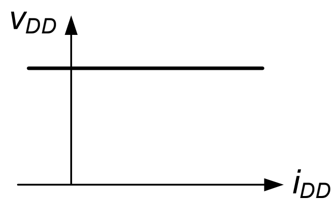
Let’s look at the components one by one…

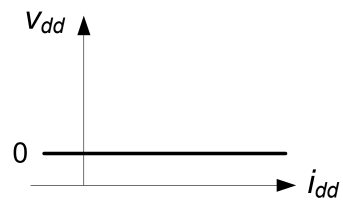
Small-signal model:



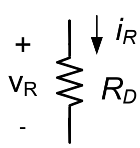
$$v_{dd} = \underbrace{\left.\frac{dv_{DD}}{di_{DD}}\right|_{i_{DD}=I_{DD}}}_{0} \cdot i_{dd}$$

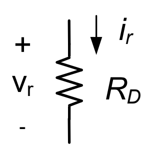




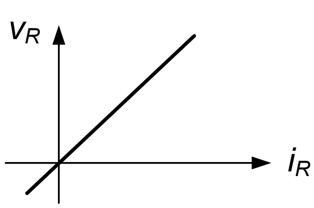


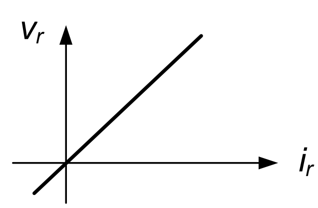
Small-signal model:





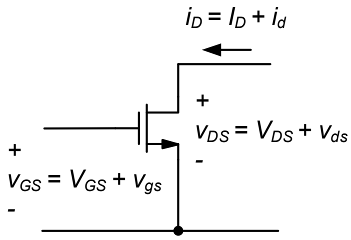
$$i_r = \left.\frac{dv_R}{di_R}\right|_{i_R=I_R} \cdot v_r = R_D \cdot v_r$$



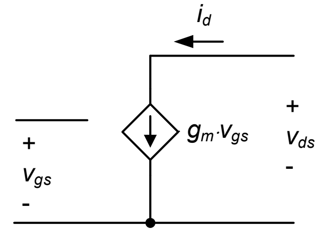


The resistor is already assumed to be linear…

Small-signal model:



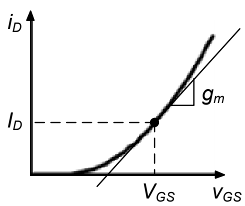
$$i_d = \frac{di_D}{dv_{GS}}\bigg|_{v_{GS}=V_{GS}} \cdot v_{gs}$$

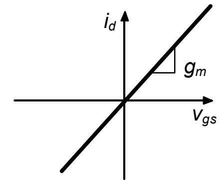


$$\frac{di_D}{dv_{GS}}\bigg|_{v_{GS}=V_{GS}} \triangleq g_m$$

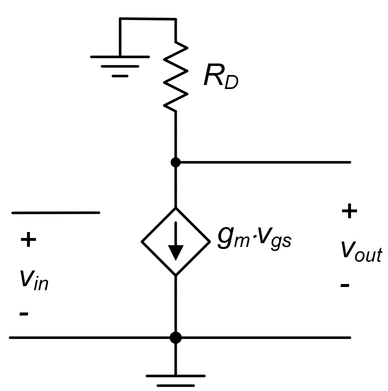
$$g_m = \frac{d}{dv_{GS}}\left[\frac{1}{2}K(v_{GS}-V_{Tn})^2\right]_{v_{GS}=V_{GS}}$$

$$g_m = K(V_{GS}-V_{Tn}) = KV_{OV}$$

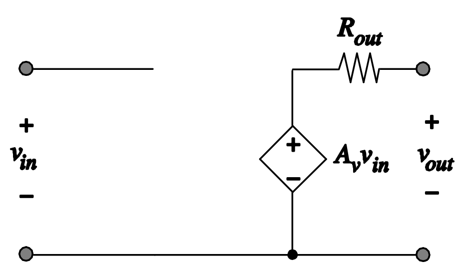




Complete Model



Voltage amplifier representation:



$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D$$

$$R_{out} = R_D$$

Other Ways to Compute g_m

$$g_m = K(V_{GS} - V_{Tn}) = KV_{OV}$$

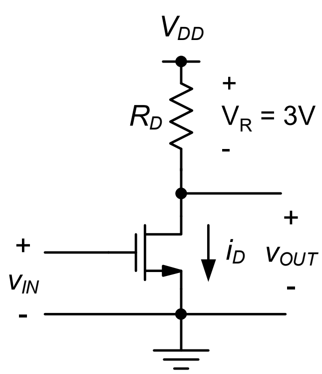
- Using the drain current equation, we can express g_m in terms of other variables

$$I_D = \frac{1}{2}KV_{OV}^2 \qquad V_{OV} = \sqrt{\frac{2I_D}{K}}$$

$$g_m = \sqrt{2KI_D}$$

$$g_m = \frac{2I_D}{V_{OV}}$$

Example 1



Transistor is biased such that

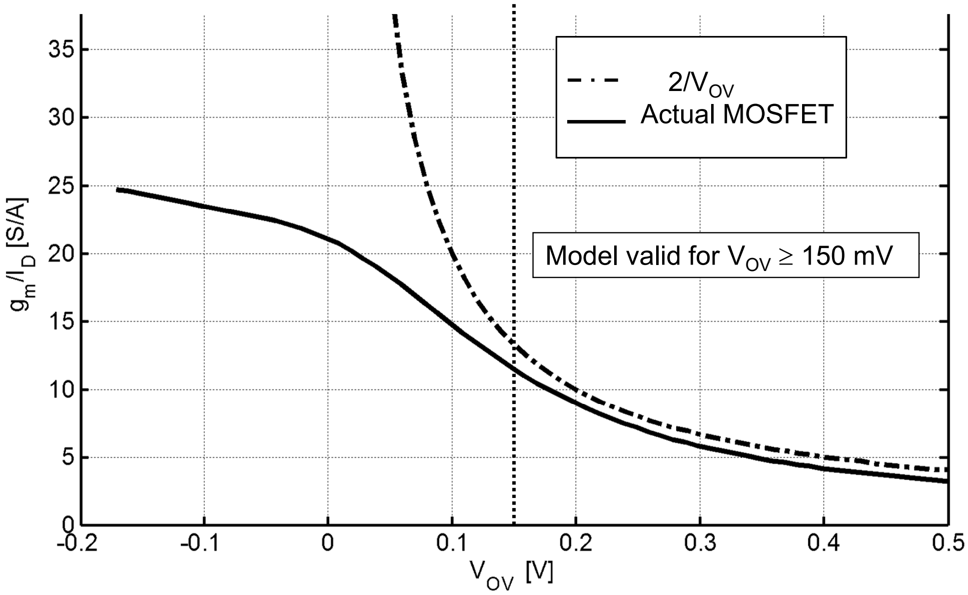
$$V_{IN} - V_{Tn} = V_{OV} = 1V$$

and the resistor is sized to have the voltage drop indicated on the left

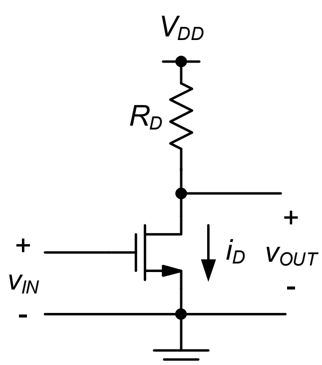
$$A_v = -g_m R_D = -\frac{2I_D}{V_{OV}}R_D = -\frac{2V_R}{V_{OV}} = -6$$

- Once the gate overdrive and the voltage drop across R_D are known, the voltage gain is fully defined
  - The "K" of the transistor does not matter at all in this situation

Does the Voltage Gain go to Infinity for $V_{OV} \rightarrow 0$?



Example 2



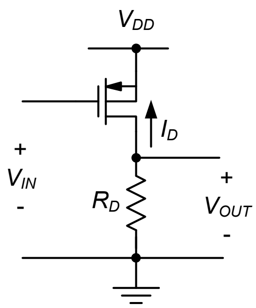
Given:

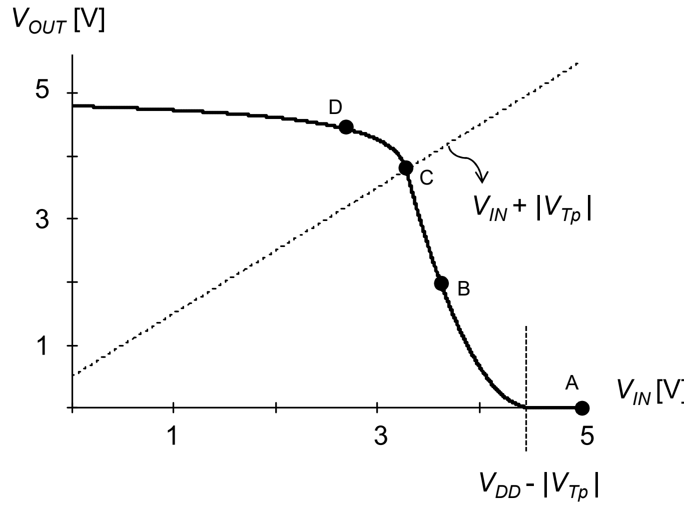
$K = 0.8\dfrac{mA}{V^2}$ $\quad V_{Tn} = 1V$ $\quad R_D = 20k\Omega$

$V_{DD} = 5V$ $\quad V_{OUT} = 3V$

- What is the required V_{IN}, what is V_{OV}?
- What is the small-signal voltage gain?

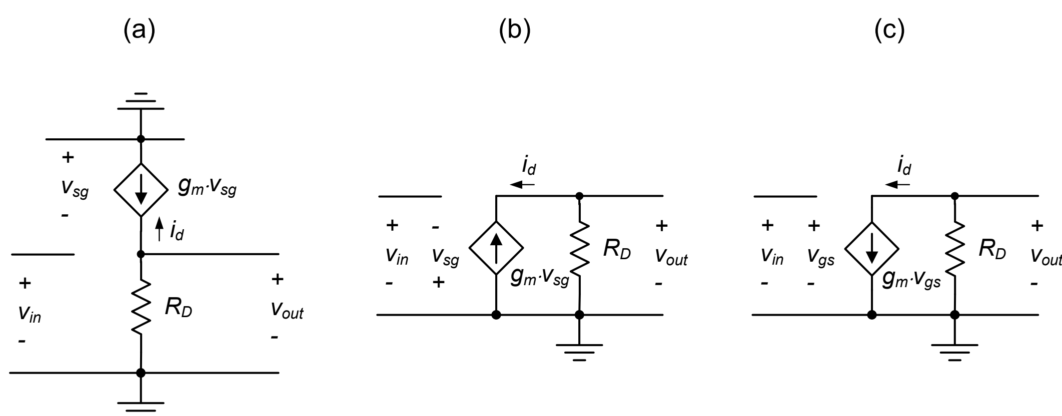
PMOS CS Stage





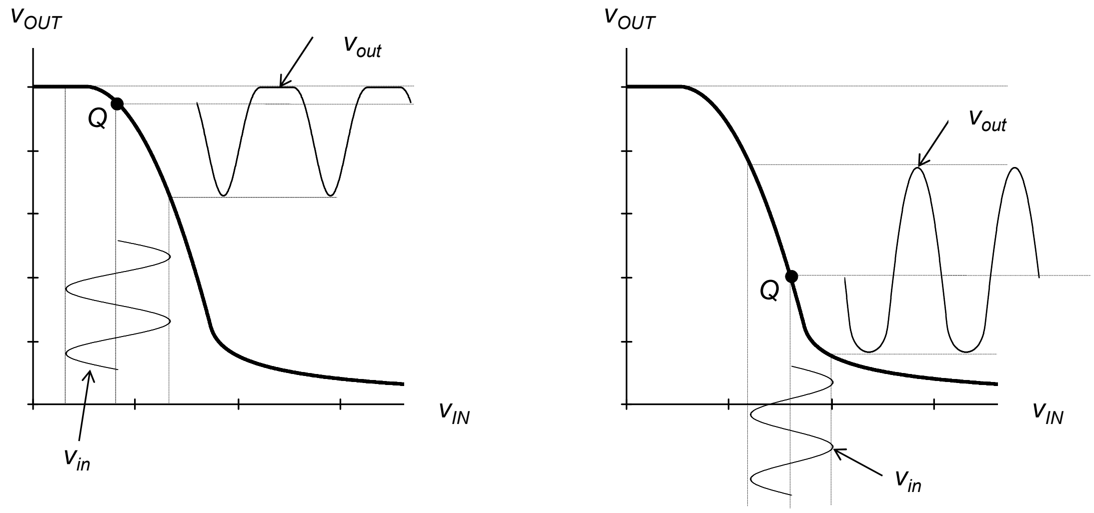
$$-I_D = \frac{1}{2} K_p (V_{SG} - |V_{Tp}|)^2$$

Small-Signal Equivalence to NMOS Circuit



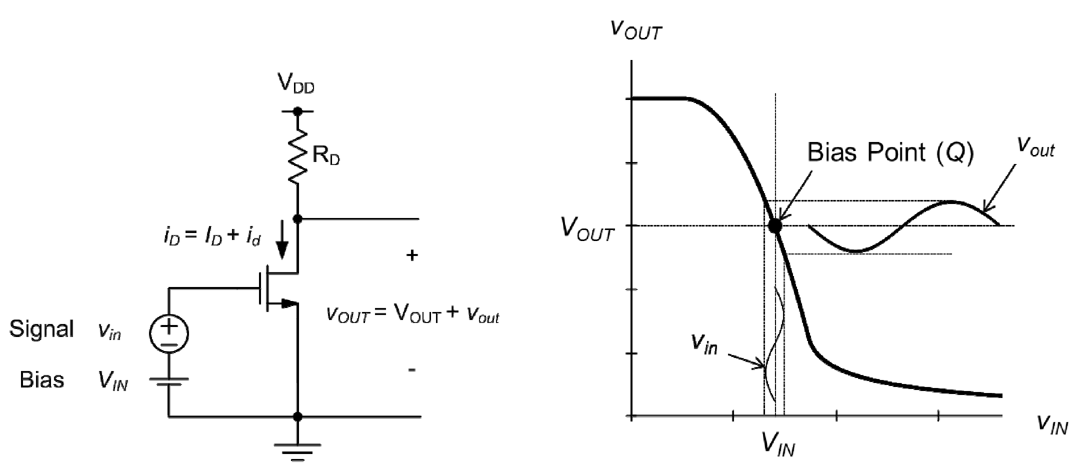
Conclusion: **Think NMOS** when it comes to the small-signal model!

Small-Signal Model Gotchas: Signal Clipping



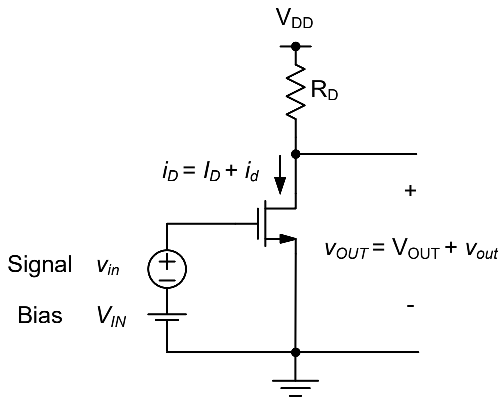
- Always be aware that the small-signal model does not tell us anything about the actual signal swings that the circuit can handle. When in doubt, go back to the large-signal model and check.

Biasing



- V_{IN} must be set accurately, so that the amplifier operates at the proper bias point

What Do We Want? — Example Re-Visited



$$V_{DD} = 5\ V$$

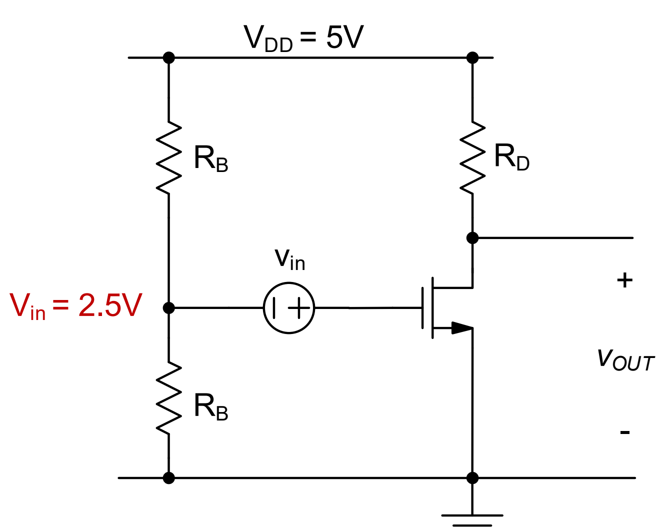
$$R_D = 10\ k\Omega,$$

$$K = 500\ \frac{\mu A}{V^2}, V_{Tn} = 1.5V$$

$$Want\quad V_{OUT} = 2.5\ V$$

$$I_D = \frac{V_{DD} - V_{OUT}}{R_D} = 0.25mA \qquad V_{IN} = V_{Tn} + V_{OV} = V_{Tn} + \sqrt{\frac{2I_D}{K}} = 2.5V$$

Possible Solution?



"Garage Electronics"

The Issue

http://www.isi.edu/~vernier/EE327/cd4007_intersil_datasheet.pdf

intersil

CD4007UBMS

November 1994

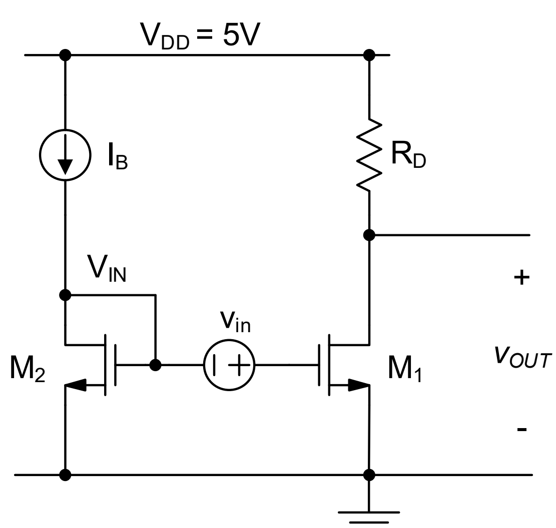
CMOS Dual Complementary Pair Plus Inverter

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1	+25°C	0.7	2.8	V

- The threshold of a MOSFET is **never** well defined
  - CD4007: V_{Tn} = 0.7…2.8V (somewhat extreme)
  - In modern IC processes, the threshold varies by about ±200mV around its nominal value – still a very large range

Replica Biasing Approach



$$V_{IN} = V_{Tn2} + \sqrt{\frac{2I_B}{K_2}} = 2.5V \qquad V_{OUT} = V_{DD} - \frac{1}{2}R_D K_1 (V_{IN} - V_{Tn1})^2$$

$$V_{OUT} = V_{DD} - \frac{1}{2} R_D K_1 \left(V_{Tn2} + \sqrt{\frac{2I_B}{K_2}} - V_{Tn1} \right)^2$$

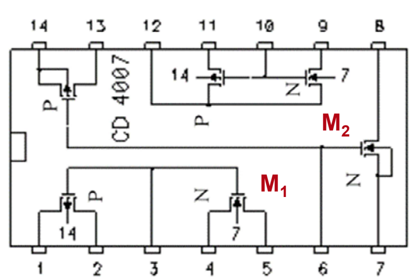
- If $K_1 = K_2$ and $V_{Tn1} = V_{Tn2}$:

$$V_{OUT} = V_{DD} - R_D I_B$$

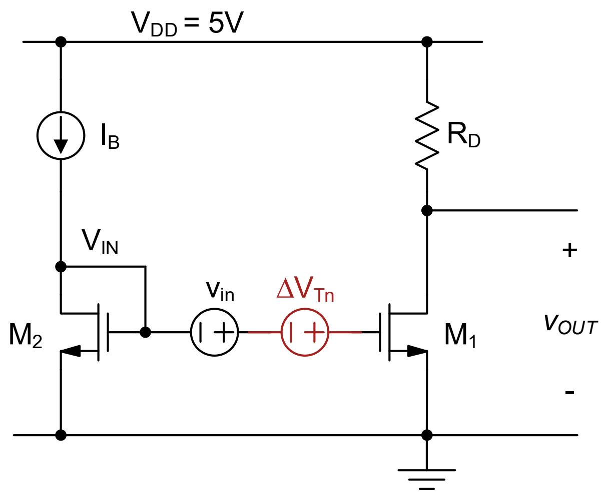
- Independent of the transistor parameters!
- In a different context (IC design), this circuit is also called a "current mirror," since $I_{D2} = I_B = I_{D1}$
  - Note that the transistors must carry the same current, since they both operate in saturation and have the same V_{GS}

Key Assumption

- For the replica bias approach to work well, the transistor parameters must match
- Luckily, this is the case for transistors in the same package
  - Since they were produced on the same wafer, at the same time, using the same manufacturing steps
- The close matching of similar components on the same chip is a property that is frequency exploited in IC design

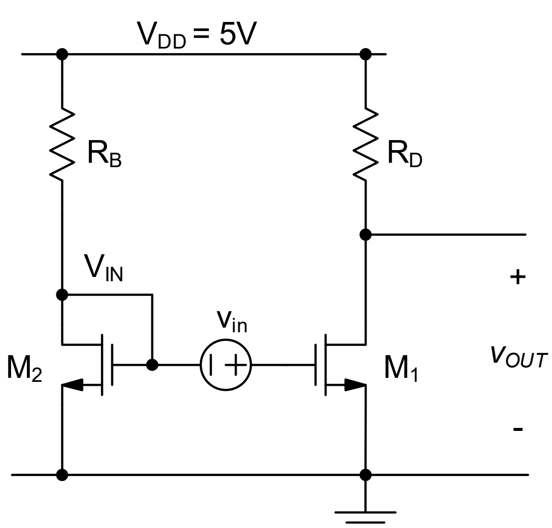


Residual Mismatch Between Devices in the Same Package



- The threshold mismatch (within a given package) for the MOSFETs we are using in the lab should be on the order of 10mV
- The difference between the thresholds can be modeled as shown above and essentially shifts the output bias point by $-A_v \cdot \Delta V_{Tn}$
  - Often not a problem

Simplified Circuit Without Current Source



- It's cumbersome to implement a current source in the lab (within the scope of what we want to do) → use a resistor instead

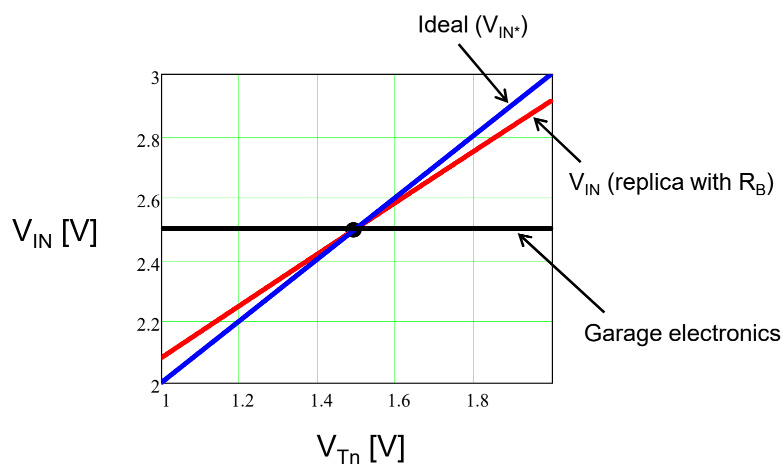
- Using this circuit, we have (see pre-lab 1)

$$V_{IN} = V_{Tn} + \frac{1}{KR_B}\left[\sqrt{1 + 2KR_B(V_{DD} - \underbrace{V_{Tn}}_{\text{undesired}})} - 1\right]$$

- Ideally, what we wanted is

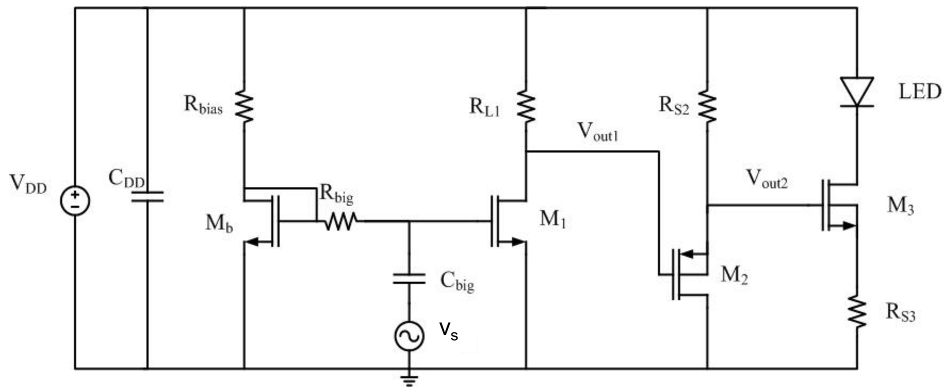
$$V_{IN^*} = V_{Tn} + \sqrt{\frac{2I_D}{K}}$$

- Suppose we pick R_B such that $V_{IN} = V_{IN^*}$ assuming nominal transistor parameters. Now, by how much does V_{IN} deviate from V_{IN^*} as V_{Tn} is varied?
- Using the numbers from the previous example:
  V_{Tn} = 1.5 V, K = 0.5 mA/V², V_{IN^*} = 2.5 V → R_B = 10kΩ



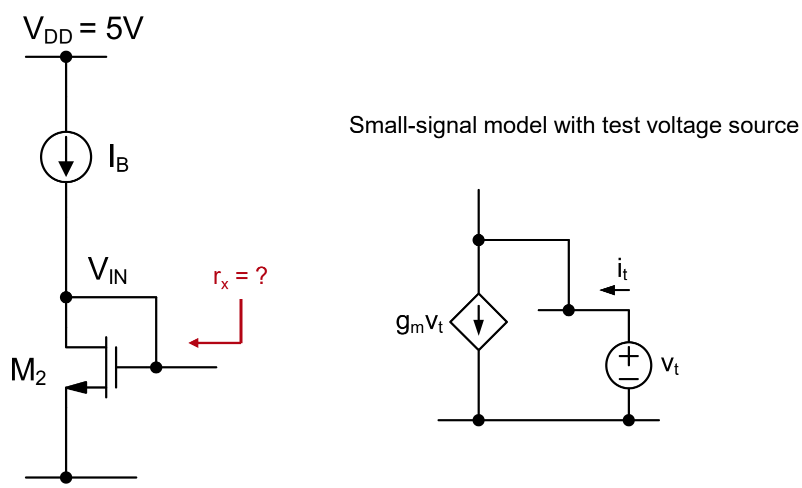
- Even though we replaced the current source with a resistor, the circuit is still quite robust
  - For a ±0.5V change in V_{Tn}, V_{IN} deviates only by about 80mV from its ideal value

Lab Transmitter Circuit



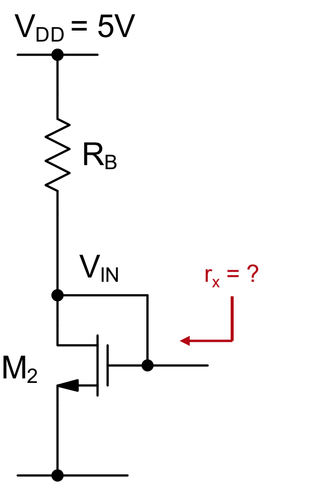
- The transmitter circuit we'll use in the lab uses the same biasing approach
- The main difference to the circuit shown previously is that we'll couple in the signal via a capacitor "C_{big}"
  - This is called "AC coupling" – more analysis to follow later
  - The main advantage is that this allows us to apply a ground referenced signal (bottom terminal of v_s connected to ground)

Small-Signal Resistance of a Diode Connected Device



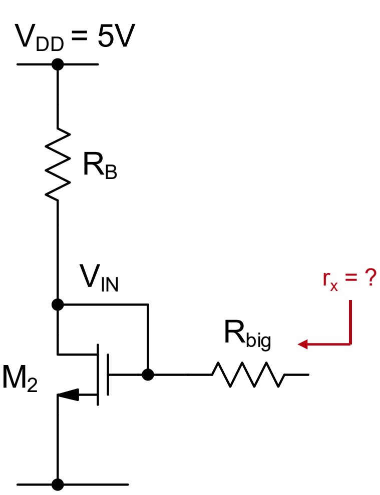
$$r_x = \frac{v_t}{i_t} = \frac{v_t}{g_m v_t} = \frac{1}{g_m}$$

Circuit with R_B



$$r_x = \frac{1}{g_m} || R_B$$

Circuit with R_{big}



Usually R_{big} >> than this term

$$r_x = \cancel{\left(\frac{1}{g_m} || R_B\right)} + R_{big}$$

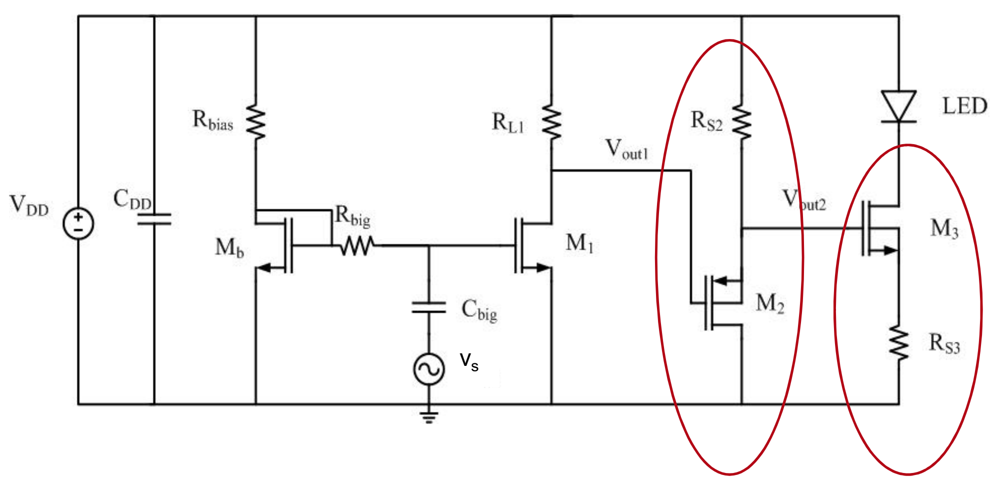
Chapter 5

The Common Drain Stage

Boris Murmann

Stanford University

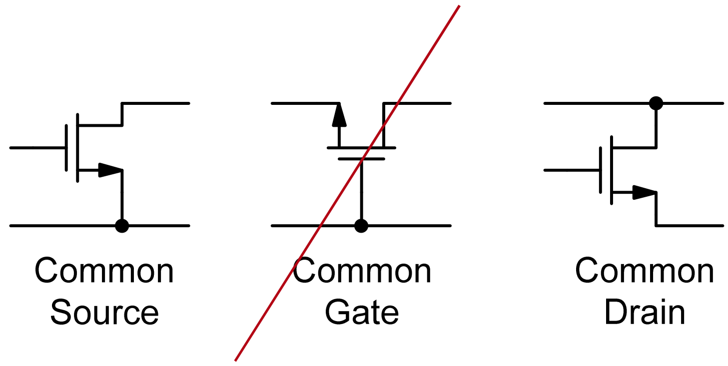
Motivation — Lab Transmitter Circuit



Common Drain Stage

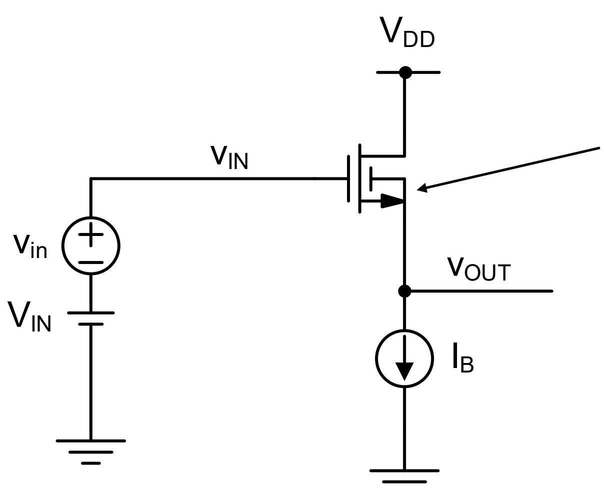
Degenerated Common Source Stage

Transistor Configurations



Not covered in EE101B

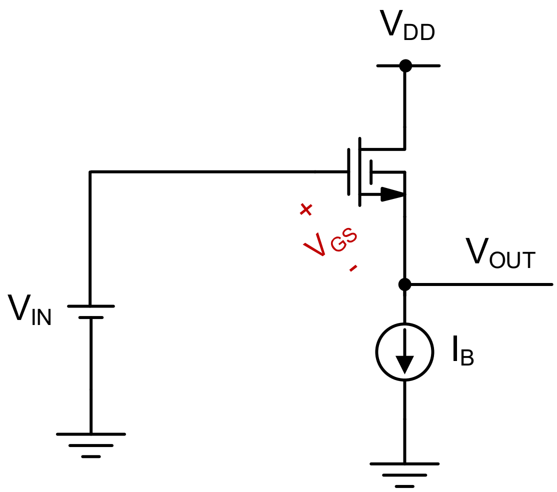
NMOS CD Stage with Ideal Current Bias



In the CD stages that we will consider, the bulk is always connected to the source.

This is not always possible (or even desirable) in IC technology (see EE114), but we can certainly do this with our 4007 parts in the lab.

DC Analysis



$$V_{GS} = V_{Tn} + \sqrt{\frac{2I_D}{K}} = constant$$

$$V_{OUT} = V_{IN} - V_{GS}$$

$$V_{DS} = V_{DD} - V_{OUT}$$

$$V_{DS} = V_{DD} - (V_{IN} - V_{GS})$$

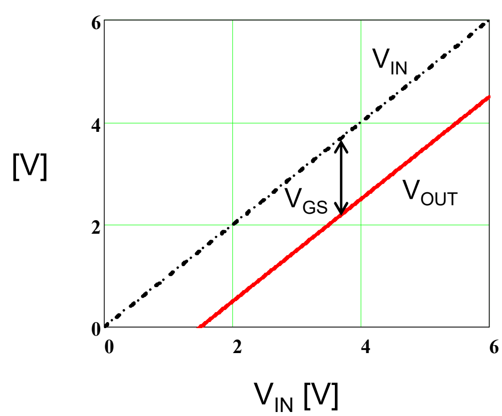
$$V_{DS} = V_{DD} - (V_{IN} - V_{Tn} - V_{OV})$$

$$V_{DS} = V_{OV} + V_{DD} + V_{Tn} - V_{IN}$$

Transistor operates in saturation unless

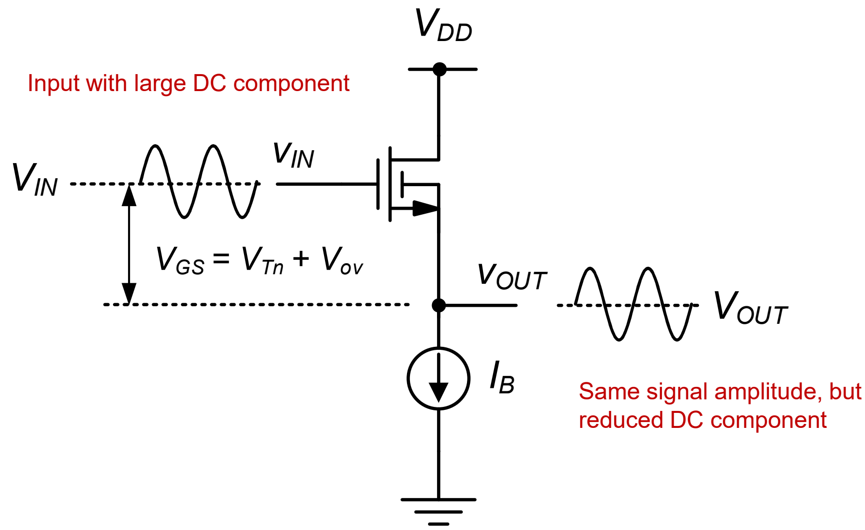
$$V_{IN} > V_{DD} + V_{Tn} > V_{DD}$$

DC Transfer Characteristic



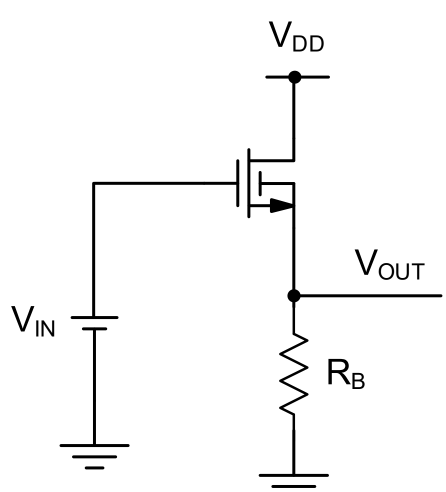
- As seen from this graph, the circuit performs a “DC level shift”
  - Exactly what we will use it for in the lab
- Since the source of the transistor directly “follows” the input, a CD stage is commonly called “source follower”

DC Level Shifting



- With the PMOS version of this circuit we can do the opposite, i.e. shift the DC level "up" instead of "down"

DC Analysis With Resistor (Instead of Current Source)



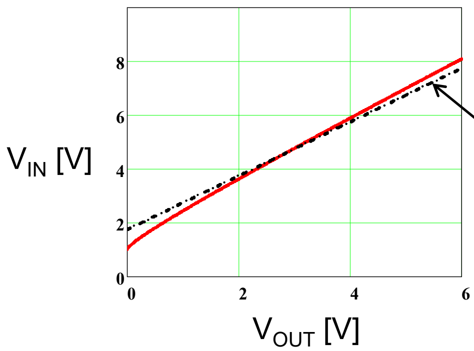
$$V_{IN} = V_{OUT} + V_{Tn} + \sqrt{\frac{2I_D}{K}}$$

$$V_{IN} = V_{OUT} + V_{Tn} + \underbrace{\sqrt{\frac{2V_{OUT}}{KR_B}}}$$

Keep this term small, by making R_B sufficiently large

Example: $$\sqrt{\frac{2 \cdot 2V}{0.5\frac{mA}{V^2} \cdot 20k\Omega}} = 200mV$$

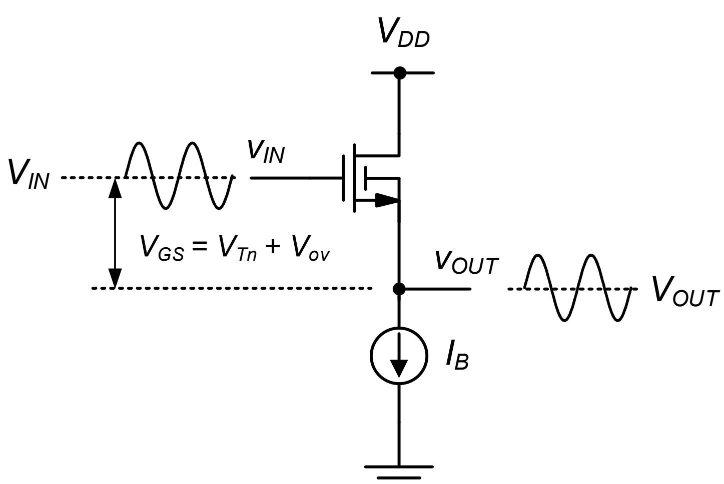
DC Transfer Characteristic with Resistor



$$V_{IN} = V_{OUT} + V_{Tn} + \sqrt{\frac{2V_{OUT}}{KR_B}}$$

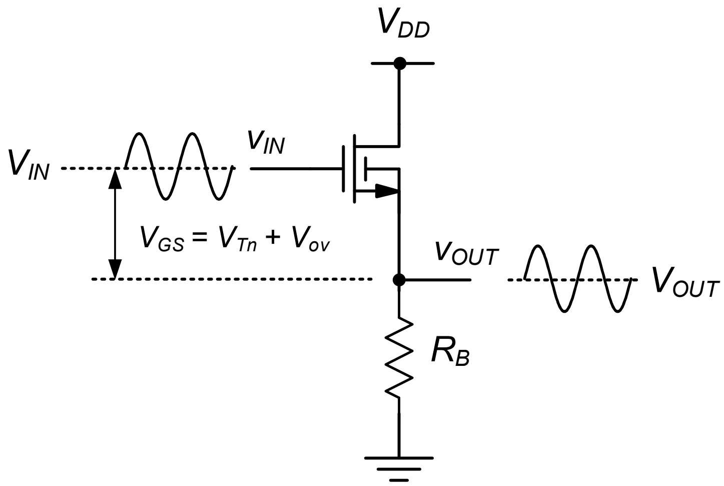
- Bottom line: If properly designed, the circuit still operates quite similar to the version with the current source

Small-Signal Analysis



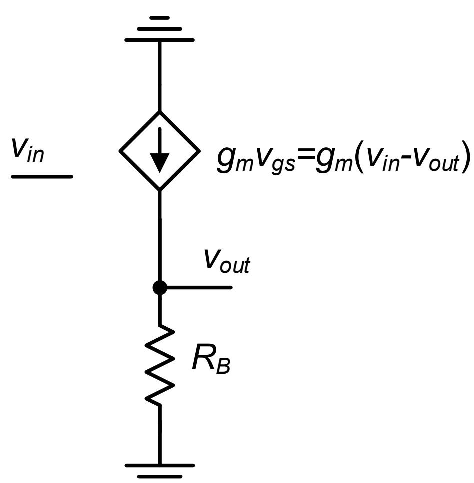
- Trivial for the circuit with current source bias: $v_{out} = v_{in} \Rightarrow A_v = \dfrac{v_{out}}{v_{in}} = 1$

Small-Signal Analysis with Resistor

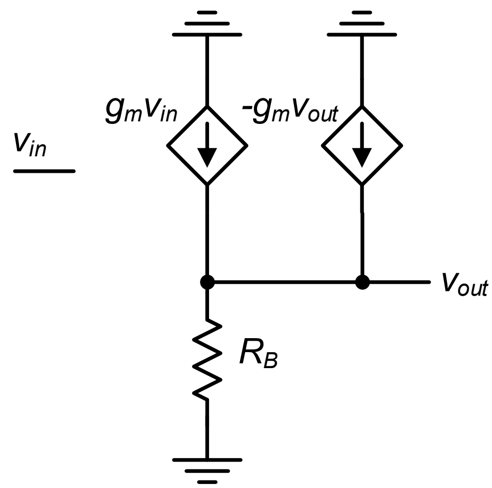


- Derive the small-signal voltage gain using the circuit's small-signal model

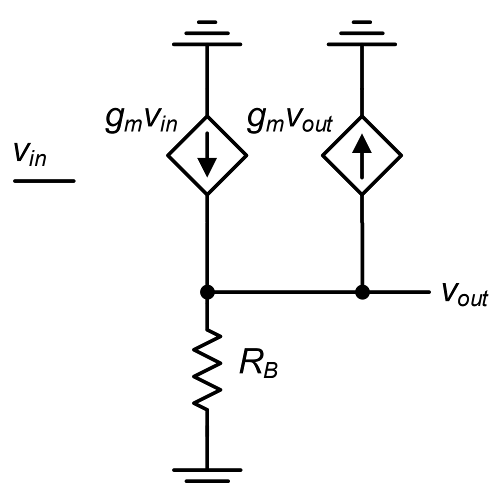
Small-Signal Analysis with Resistor



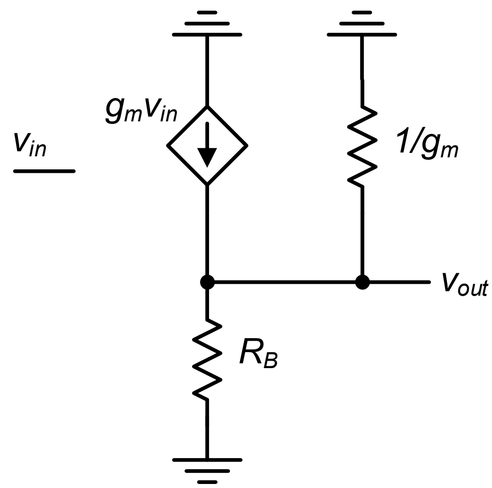
- From here, we could simply grind through KCL to get the result, but we can gain better intuition by "massaging" the circuit a little bit…



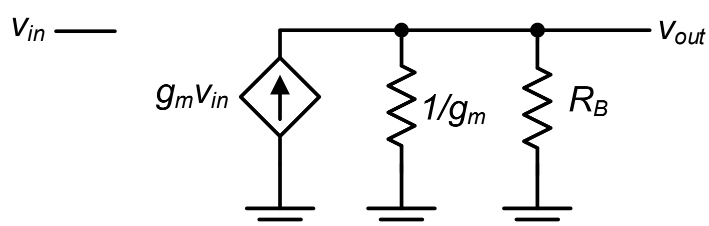
v_{in}
$g_m v_{in}$
$-g_m v_{out}$
v_{out}
R_B



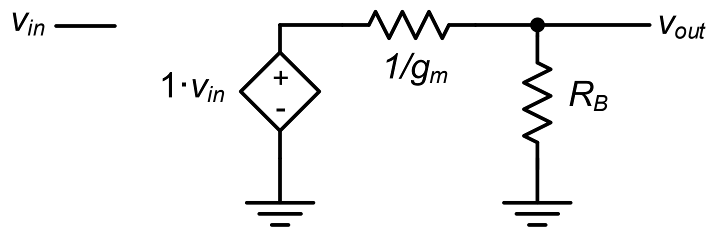
v_{in}
$g_m v_{in}$
$g_m v_{out}$
v_{out}
R_B



Drawn A Bit More Nicely…

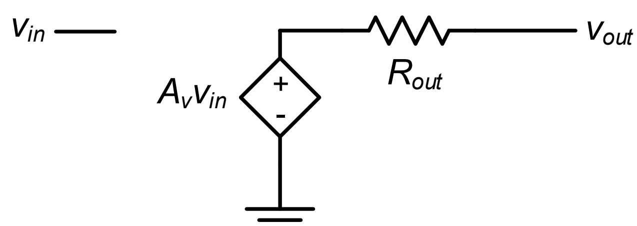


- The output resistance of the CD stage is low (since $1/g_m$ is typically just a few hundred ohms or less in our circuits)



- Without R_B the voltage gain would be exactly unity
  - As we already know

Final Model

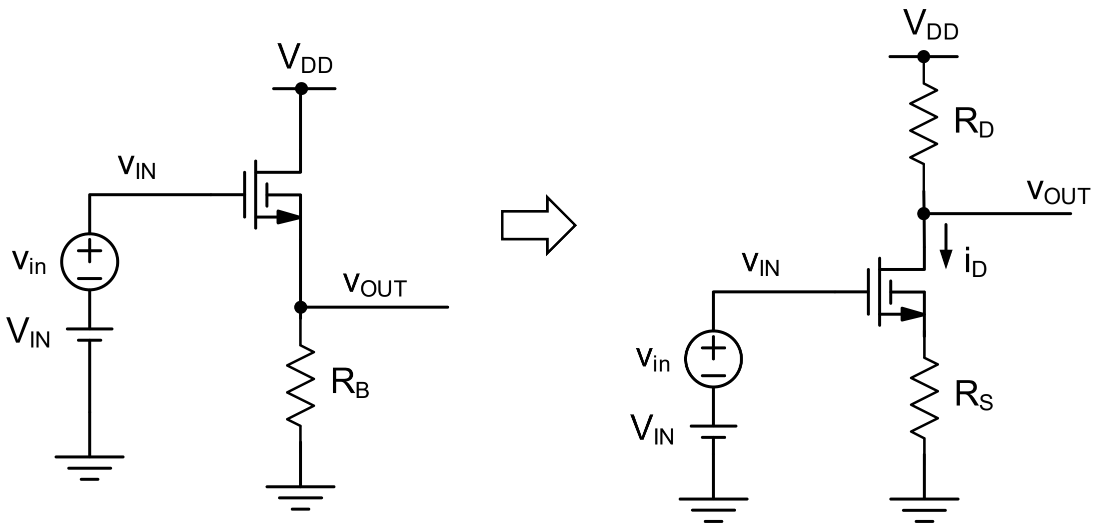


$$A_v = \frac{R_B}{R_B + \frac{1}{g_m}} = \frac{g_m R_B}{1 + g_m R_B} \cong 1 \quad for\ g_m R_B \gg 1$$

Example: $2mS \cdot 10k\Omega = 20$

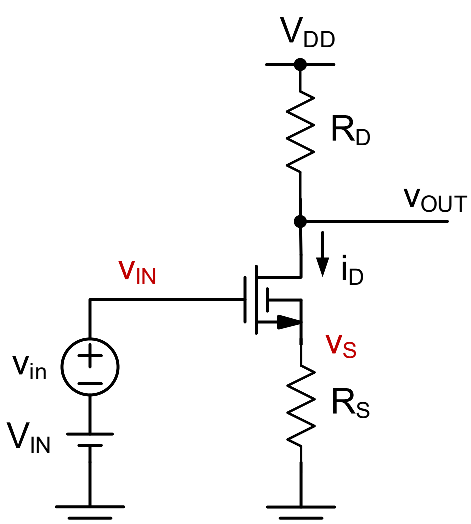
$$R_{out} = \frac{1}{g_m} || R_B = \frac{\frac{1}{g_m} \cdot R_B}{R_B + \frac{1}{g_m}} = \frac{1}{g_m} \frac{g_m R_B}{1 + g_m R_B} \cong \frac{1}{g_m} \quad for\ g_m R_B \gg 1$$

CD Stage → Source Degenerated CS Stage



- Very similar, except that we take the output at the drain

Small-Signal Analysis



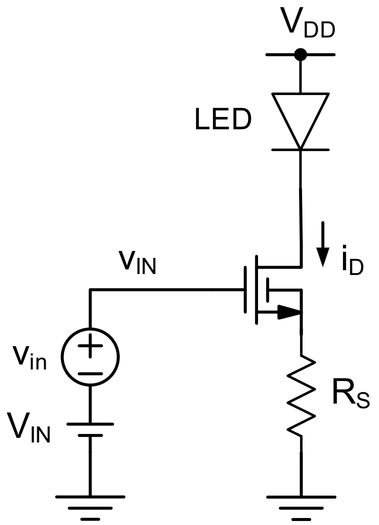
Provided that the transistor operates in saturation, we know from our CD stage analysis:

$$v_s = \frac{g_m R_S}{1 + g_m R_S} v_{in}$$

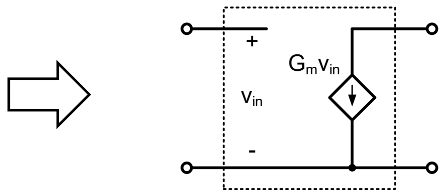
$$i_d = \frac{v_s}{R_S} = \frac{g_m}{1 + g_m R_S} v_{in} \cong \frac{1}{R_S} v_{in}$$

$$v_o = -i_d R_D = -\frac{g_m R_D}{1 + g_m R_S} v_{in} \cong -\frac{R_D}{R_S} v_{in}$$

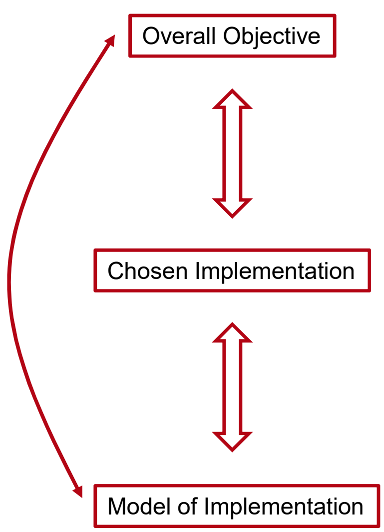
Using the Degenerated CS Stage as a Transconductance Amplifier

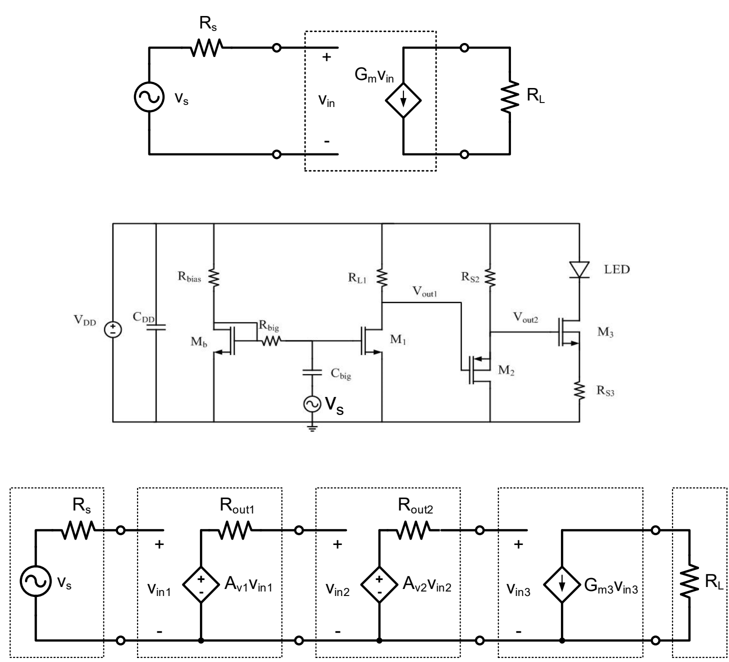


$$G_m = \frac{i_d}{v_{in}} = \frac{g_m}{1 + g_m R_S} \cong \frac{1}{R_S}$$



Putting It All Together…





Chapter 6

RLC & LTI review

Boris Murmann

Stanford University

References: E40 or EE101A textbooks (any), EE102A lecture notes

Capacitor

Passive element that stores energy in electric field

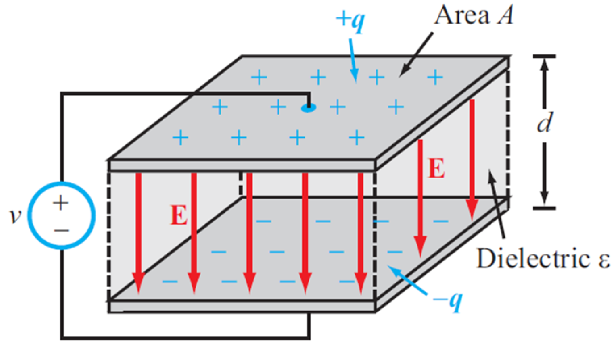
$$i = C\frac{dv}{dt} \qquad q = Cv$$

$$v = \frac{1}{C}\int_{t_0}^{t} i\,dt + v(t_0)$$

- For DC, capacitor looks like open circuit
- Voltage on capacitor must be continuous (no abrupt change)

Parallel plate capacitor

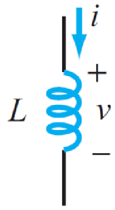
$$C = \frac{\varepsilon A}{d}$$



[Ulaby & Maharbiz]

Inductor

Passive element that stores energy in magnetic field



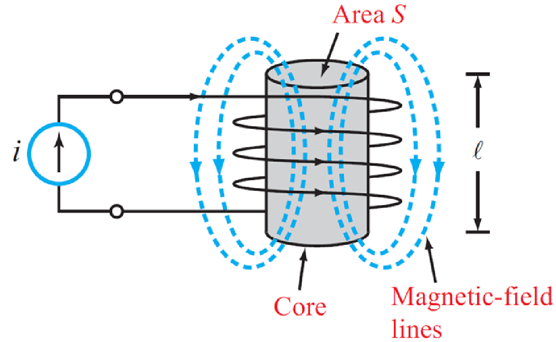
$$v = L\frac{di}{dt}$$

$$i = \frac{1}{L}\int_{t_0}^{t} v(t)\,dt + i(t_0)$$

- At dc, inductor looks like a short circuit
- Current through inductor must be continuous (no abrupt change)

$$w = \frac{1}{2}Li^2 \qquad \text{(J)},$$

Solenoid Wound Inductor



[Ulaby & Maharbiz]

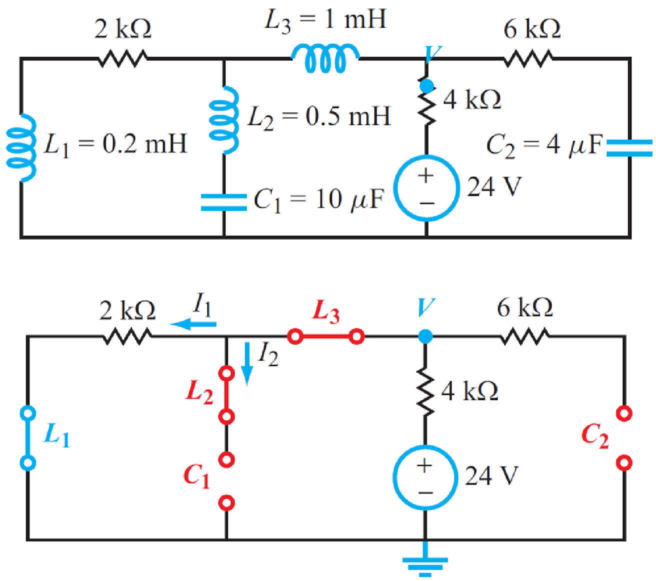
$$L = \frac{N^2\mu A}{l}$$

[Ulaby & Maharbiz]

Table 5-4: Basic properties of R, L, and C.

Property	R	L	C
i–v relation	$i = \frac{v}{R}$	$i = \frac{1}{L}\int_{t_0}^{t} v\,dt + i(t_0)$	$i = C\frac{dv}{dt}$
v-i relation	$v = iR$	$v = L\frac{di}{dt}$	$v = \frac{1}{C}\int_{t_0}^{t} i\,dt + v(t_0)$
p (power transfer in)	$p = i^2R$	$p = Li\frac{di}{dt}$	$p = Cv\frac{dv}{dt}$
w (stored energy)	0	$w = \frac{1}{2}Li^2$	$w = \frac{1}{2}Cv^2$
Series combination	$R_{\text{eq}} = R_1 + R_2$	$L_{\text{eq}} = L_1 + L_2$	$C_{\text{eq}} = \frac{C_1C_2}{C_1 + C_2}$
Parallel combination	$R_{\text{eq}} = \frac{R_1R_2}{R_1 + R_2}$	$L_{\text{eq}} = \frac{L_1L_2}{L_1 + L_2}$	$C_{\text{eq}} = C_1 + C_2$
dc behavior	no change	short circuit	open circuit
Can v change instantaneously?	yes	yes	no
Can i change instantaneously?	yes	no	yes

RLC Circuit at DC



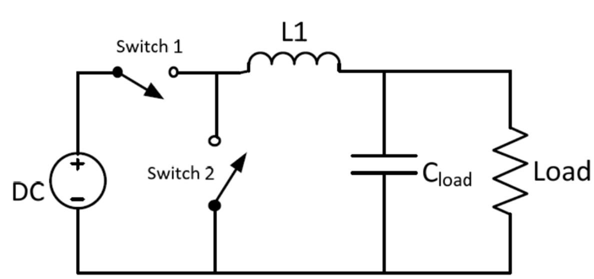
V = ?

[Ulaby & Maharbiz]

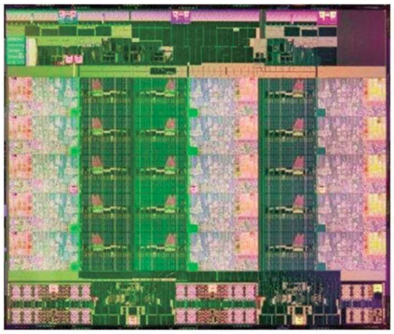
The Role of L and C in Practical Circuits

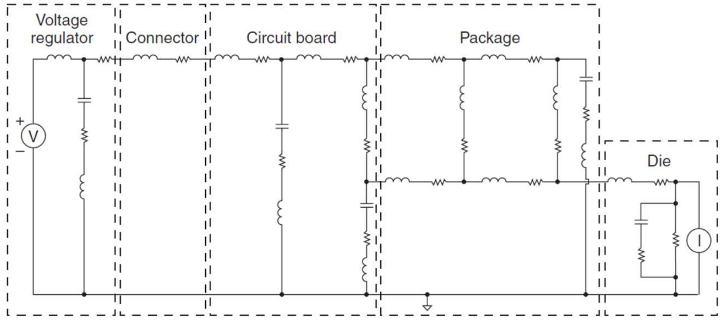
- Sometimes your friend, sometimes your foe
  - In some circuits we exploit the energy storage nature and add explicit L and C to achieve a certain objective
  - In some circuits, we are limited by the unwanted presence of L and/or C → Parasitic capacitance, parasitic inductance

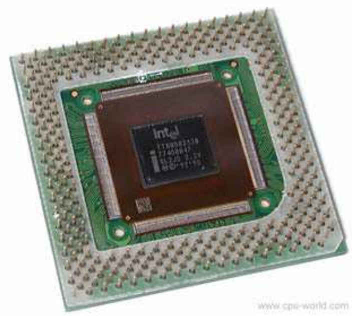
Example:
EE101A DC-DC converter

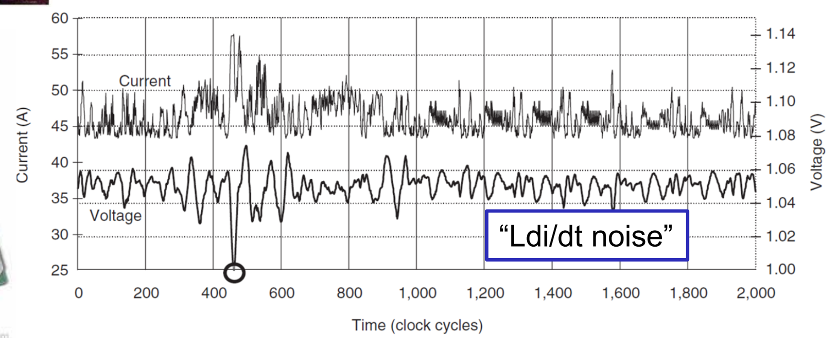


Example: Microprocessor Power Supply





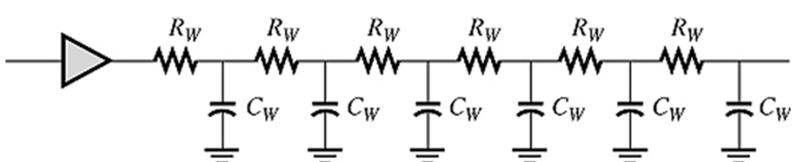




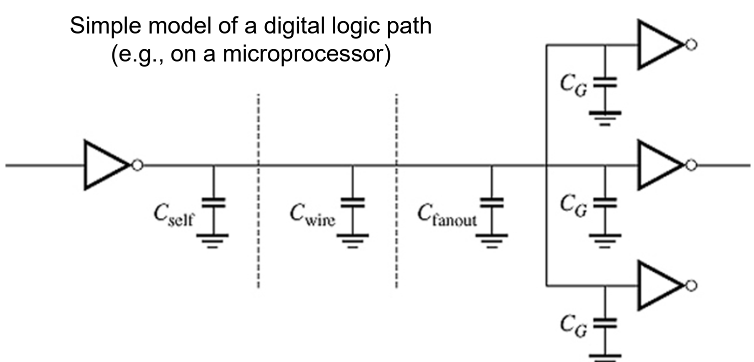
[Grochowski et al, "Microarchitectural di/dt Control," IEEE Design & Test of Computers, May-June 2003]

Example: Wire Delay and Gate Delay

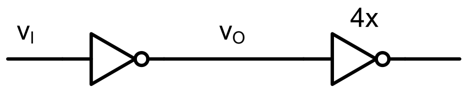
Simple model of a long wire (e.g., on a microprocessor)

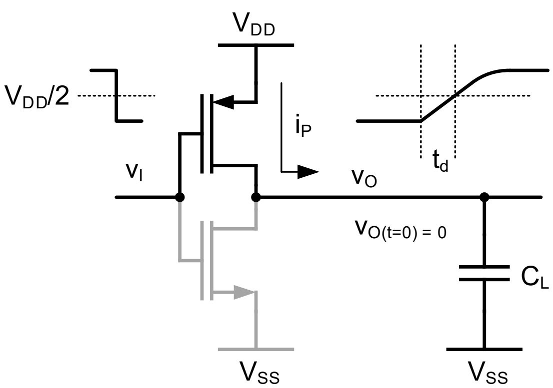


Simple model of a digital logic path
(e.g., on a microprocessor)



(Cheesy) Analysis of Digital Logic Delay





$$i_P = C_L \frac{dv_O}{dt}$$

$$t_d = \frac{V_{DD}/2}{\frac{dv_O}{dt}} = \frac{1}{2}\frac{C_L V_{DD}}{i_P}$$

$$C_L \cong 4(C_{gn} + C_{gp}) \cong 8 \cdot WLC_{ox}$$

$$i_P \cong \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{DD} - |V_{Tp}|\right)^2$$

$$t_d = \frac{1}{2}\frac{C_L V_{DD}}{i_P} \cong \frac{1}{2}\frac{8 \cdot WLC_{ox}V_{DD}}{\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{Tp}\right)^2}$$

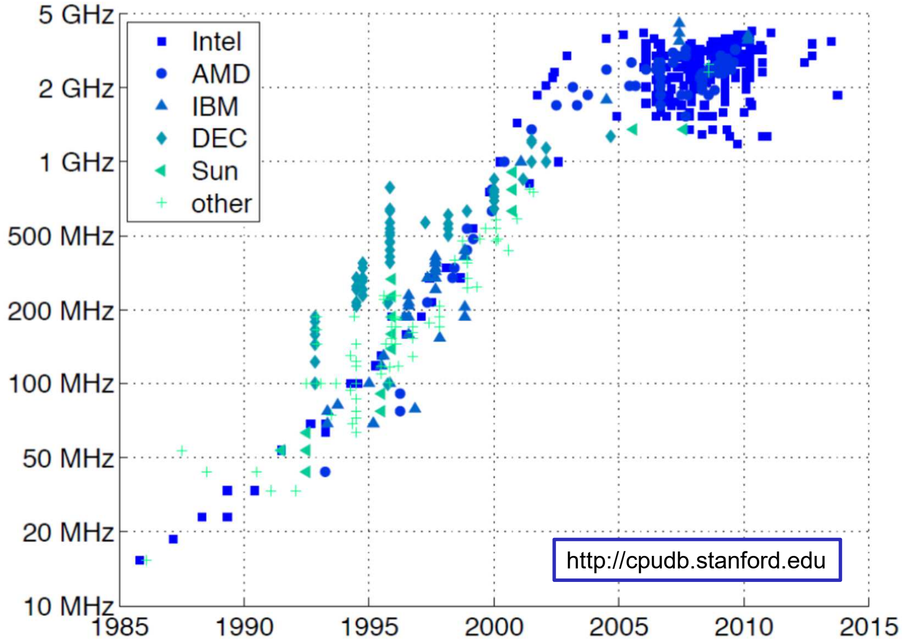
$$t_d \cong \frac{8L^2 V_{DD}}{\mu\left(V_{DD} - V_{Tp}\right)^2} \boxed{\cong \frac{8L^2}{\mu V_{DD}}}$$

Example: $$t_d \cong \frac{8(1\mu m)^2}{100\frac{cm^2}{Vs} \cdot 5V} = 160ps$$

- Assuming that we need to accommodate 10 such delays within each processor cycle, this leads to a clock speed of

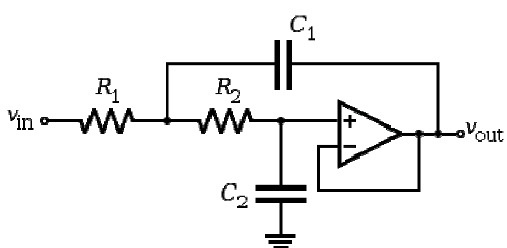
$$f_{CLK} \cong \frac{1}{10 \cdot 160ps} = 625MHz$$

Microprocessor Clock Speed Over Time

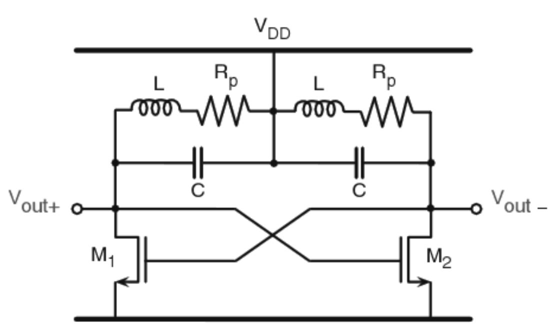


Example: Analog Filters, Oscillators

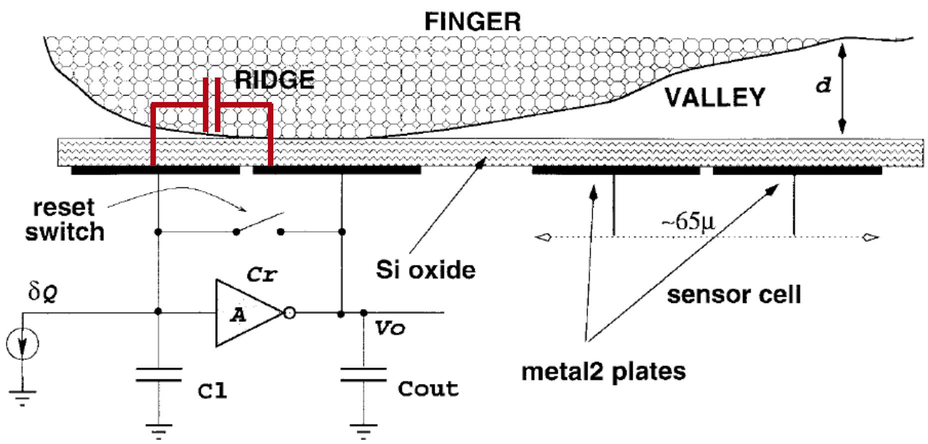
Sallen-Key
Lowpass filter



LC Oscillator



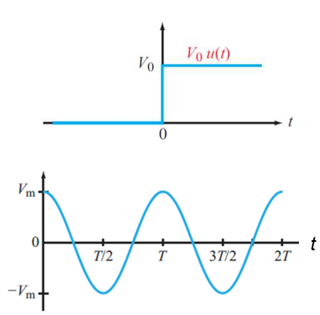
Example: Fingerprint Sensor

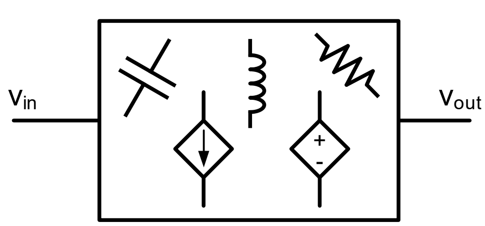


[Tartagni, IEEE J. Solid-State Circuits, Jan. 1998]

What Do We Want to Accomplish?

- For arbitrary systems consisting of R, L, C and controlled sources
  - Predict the response to practically relevant signals
    - Steps, ramps, sinusoids, stepped sinusoids, …
  - Describe the system itself in a compact and insightful way
    - Poles and zeros (more later)





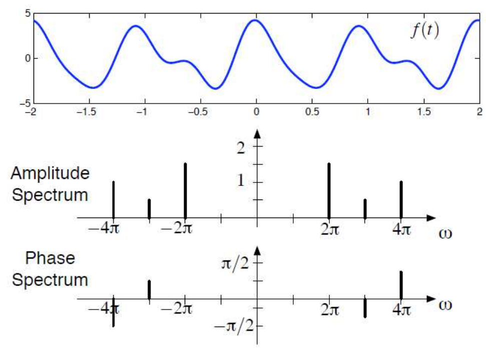
Why Sinusoids?

- We can decompose arbitrary periodic signals into sums of sinusoids
  - Fourier series, see EE102A

$$f(t) = \sum_{n=-\infty}^{\infty} D_n e^{jn\omega_0 t} \qquad D_n = \frac{1}{T_0}\int_{\tau}^{\tau+T_0} f(t)e^{-jn\omega_0 t}\,dt$$

$$f(t) = 3\cos(2\pi t) + \cos(3\pi t - \pi/4) + 2\cos(4\pi t + \pi/3)$$

Example:

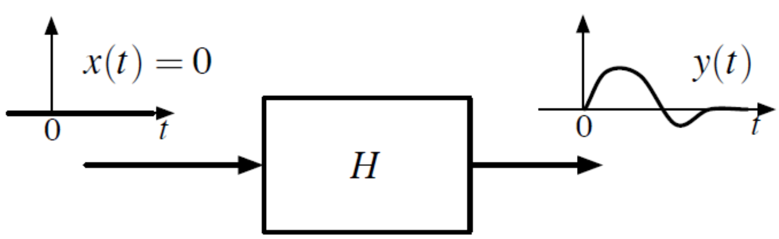


[Pauly, EE102A]

LTI Review: Response of a System (in General)

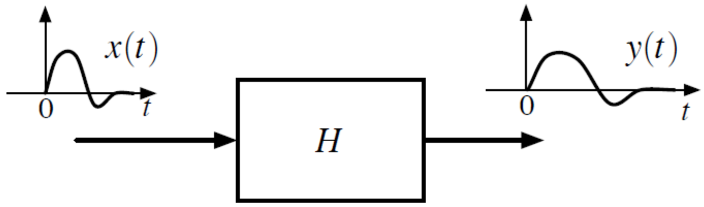
The output consists of two components:

- The *zero-input* response, which is what the system does with no input at all. This is due to initial conditions, such as energy stored in capacitors and inductors.

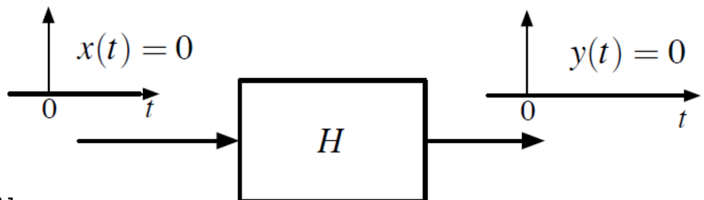


[Pauly, EE102A]

- The *zero-state* response, which is the output of the system with all initial conditions zero.

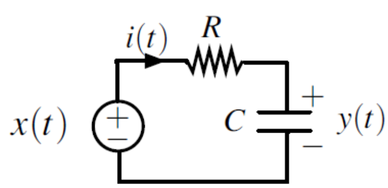


If H is a linear system, its zero-input response is zero. Homogeneity states if $y = F(ax)$, then $y = aF(x)$. If $a = 0$ then a zero input requires a zero output.



[Pauly, EE102A]

Example: Solve for the voltage across the capacitor $y(t)$ for an arbitrary input voltage $x(t)$, given an initial value $y(0) = Y_0$.



[Pauly, EE102A]

From Kirchhoff's voltage law

$$x(t) = Ri(t) + y(t)$$

Using $i(t) = Cy'(t)$

$$RCy'(t) + y(t) = x(t).$$

This is a first order LCCODE, which is linear with zero initial conditions. First we solve for the homogeneous solution by setting the right side (the input) to zero

$$RCy'(t) + y(t) = 0.$$

The solution to this is

$$y(t) = Ae^{-t/RC}$$

which can be verified by direct substitution.

To solve for the total response, we let the undetermined coefficient be a function of time

$$y(t) = A(t)e^{-t/RC}.$$

Substituting this into the differential equation

$$RC\left[A'(t)e^{-t/RC} - \frac{1}{RC}A(t)e^{-t/RC}\right] + A(t)e^{-t/RC} = x(t)$$

Simplying

$$A'(t) = x(t)\left[\frac{1}{RC}e^{t/RC}\right]$$

which can be integrated from $t = 0$ to get

$$A(t) = \int_0^t x(\tau)\left[\frac{1}{RC}e^{\tau/RC}\right]d\tau + A(0)$$

[Pauly, EE102A]

Then

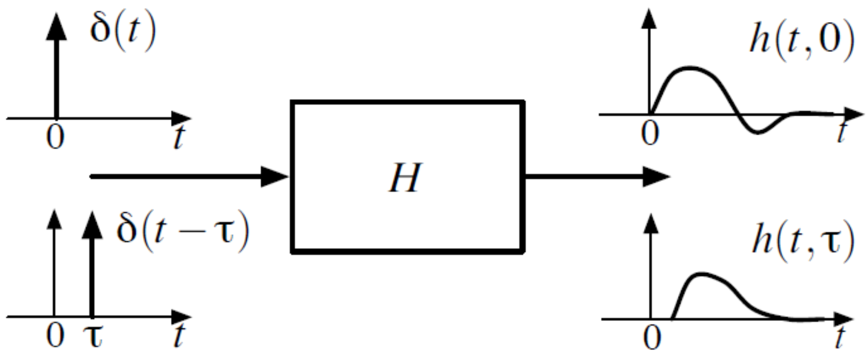
$$\begin{aligned} y(t) &= A(t)e^{-t/RC} \\ &= e^{-t/RC}\int_0^t x(\tau)\left[\frac{1}{RC}e^{\tau/RC}\right]d\tau + A(0)e^{-t/RC} \\ &= \int_0^t x(\tau)\left[\frac{1}{RC}e^{-(t-\tau)/RC}\right]d\tau + A(0)e^{-t/RC} \end{aligned}$$

At $t = 0$, $y(0) = Y_0$, so this gives $A(0) = Y_0$

$$y(t) = \underbrace{\int_0^t x(\tau)\left[\frac{1}{RC}e^{-(t-\tau)/RC}\right]d\tau}_{\text{zero}-\text{state response}} + \underbrace{Y_0 e^{-t/RC}}_{\text{zero}-\text{input response}}.$$

[Pauly, EE102A]

Impulse Response



If H is time invariant (true for almost all circuits we deal with in EE101B):

$$h(t) = H(\delta(t))$$

[Pauly, EE102A]

RC Circuit Impulse Response

Let Y_0=0, and x(t) = δ(t).

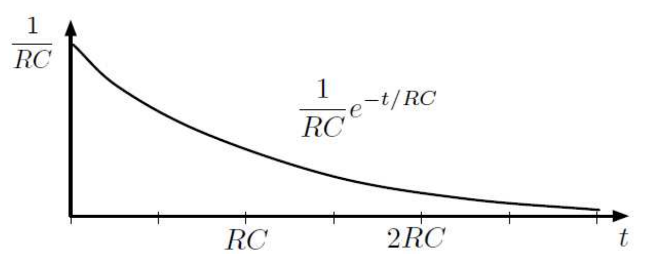
$$\begin{aligned} h(t) &= \int_{0-}^{t} \delta(\tau) \left[\frac{1}{RC} e^{-(t-\tau)/RC} \right] d\tau \\ &= \frac{1}{RC} e^{-t/RC} \end{aligned}$$

Recall that:

$$\int_{-\infty}^{\infty} f(t)\delta(t-T)\, dt = f(T)$$

for $t \geq 0$, and zero otherwise. We integrate from $0-$ to include the impulse.

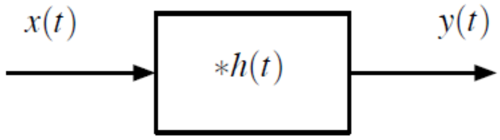
This impulse response looks like:



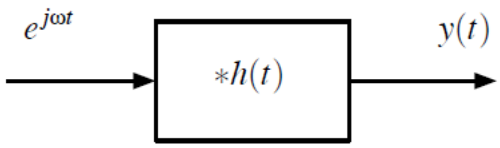
[Pauly, EE102A]

For an LTI system with impulse response $h(t)$, output is the convolution of input and impulse response:

$$y(t) = \int_{-\infty}^{\infty} h(\tau)x(t-\tau)\,d\tau$$



If the input is a complex exponential $x(t) = e^{j\omega t}$



[Pauly, EE102A]

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h(\tau)e^{j\omega(t-\tau)}\,d\tau \\ &= e^{j\omega t}\int_{-\infty}^{\infty} h(\tau)e^{-j\omega\tau}\,d\tau \triangleq H(j\omega)e^{j\omega t} \end{aligned}$$

- Complex exponential in $\Rightarrow$
  same complex exponential $\times$ complex constant out,
- Complex exponential is *eigenfunction* of LTI system with *eigenvalue* $H(j\omega)$

- $H(j\omega)$ is the continuous time Fourier transform of h(t)
- The Fourier transform allows us to replace the convolution operation by a simple multiplication
- General definition of the continuous time Fourier transform

$$F(j\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt$$

Computing the System Output Using the Fourier Transform

$$Y(j\omega) = H(j\omega)X(j\omega)$$

where $X(j\omega)$ is the input spectrum, $Y(j\omega)$ is the output spectrum, and $H(j\omega)$ is the Fourier transform of the impulse response $h(t)$.

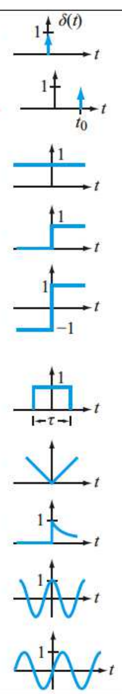
- $H(j\omega)$ is called the *frequency response* or *transfer function* of the system. Each frequency in the input spectrum $X(j\omega)$ is
  - Scaled by the *system amplitude response* $|H(j\omega)|$,

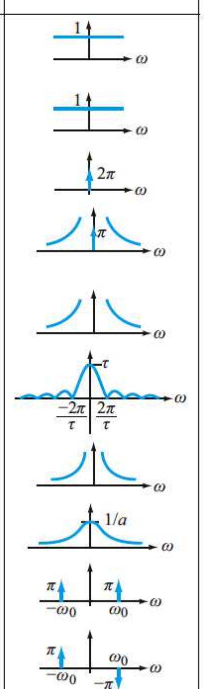
$$|Y(j\omega)| = |H(j\omega)||X(j\omega)|$$

  - Phase shifted by the *system phase response* $\angle H(j\omega)$,

$$\angle Y(j\omega) = \angle H(j\omega) + \angle X(j\omega)$$

[Pauly, EE102A]





	$f(t)$		$\mathbf{F}(\omega) = \mathcal{F}[f(t)]$
	BASIC FUNCTIONS		
1.	$\delta(t)$	↔	1
1a.	$\delta(t-t_0)$	↔	$e^{-j\omega t_0}$
2.	1	↔	$2\pi\,\delta(\omega)$
3.	$u(t)$	↔	$\pi\,\delta(\omega) + 1/j\omega$
4.	$\mathrm{sgn}(t)$	↔	$2/j\omega$
5.	$\mathrm{rect}(t/\tau)$	↔	$\tau\,\mathrm{sinc}(\omega\tau/2)$
6.	$\lvert t\rvert$	↔	$-2/\omega^2$
7.	$e^{-at}\,u(t)$	↔	$1/(a+j\omega)$
8.	$\cos\omega_0 t$	↔	$\pi[\delta(\omega-\omega_0)+\delta(\omega+\omega_0)]$
9.	$\sin\omega_0 t$	↔	$j\pi[\delta(\omega+\omega_0)-\delta(\omega-\omega_0)]$
	ADDITIONAL FUNCTIONS		
10.	$e^{j\omega_0 t}$	↔	$2\pi\,\delta(\omega-\omega_0)$
11.	$te^{-at}\,u(t)$	↔	$1/(a+j\omega)^2$
12.	$[e^{-at}\sin\omega_0 t]\,u(t)$	↔	$\omega_0/[(a+j\omega)^2+\omega_0^2]$
13.	$[e^{-at}\cos\omega_0 t]\,u(t)$	↔	$(a+j\omega)/[(a+j\omega)^2+\omega_0^2]$

Fourier Transform Pairs

($a \geq 0$)

[Ulaby & Maharbiz]

- If the input is to a system is a complex exponential $e^{j\omega_0 t}$, the input spectrum is

$$\begin{aligned} X(j\omega) &= \mathcal{F}\left[e^{j\omega_0 t}\right] \\ &= 2\pi\delta(\omega - \omega_0). \end{aligned}$$

The output spectrum is

$$\begin{aligned} Y(j\omega) &= H(j\omega)(2\pi\delta(\omega - \omega_0)) \\ &= H(j\omega_0)(2\pi\delta(\omega - \omega_0)). \end{aligned}$$

The ouput signal is

$$\begin{aligned} y(t) &= \mathcal{F}^{-1}\left[Y(j\omega)\right] \\ &= \mathcal{F}^{-1}\left[H(j\omega_0)(2\pi\delta(\omega - \omega_0))\right] \end{aligned}$$

[Pauly, EE102A]

$$\begin{aligned} &= H(j\omega_0)e^{j\omega_0 t} \\ &= |H(j\omega_0)|e^{j(\omega_0 t + \angle H(j\omega_0))} \end{aligned}$$

A sinusoidal input $e^{j\omega_0 t}$ to an LTI system produces a sinusoidal output at the

- Same frequency,
- Scaled in amplitude, and
- Phase shifted.

This corresponds to multiplication by a complex number $H(j\omega_0)$.

[Pauly, EE102A]

Important Expressions

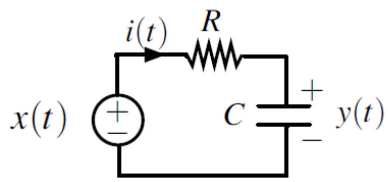
$$e^{j\omega t} = \cos(\omega t) + j \cdot sin(\omega t)$$

$$\cos(\omega t) = \frac{1}{2}\left(e^{j\omega t} + e^{-j\omega t}\right)$$

$$\sin(\omega t) = \frac{1}{2j}\left(e^{j\omega t} - e^{-j\omega t}\right)$$

(Note that these expressions clarify the relationship between transform pairs 8, 9, 10)

Back to Our RC Circuit



$$h(t) = \frac{1}{RC} e^{-\frac{t}{RC}} \cdot u(t) \quad \overset{}{\underset{(7)}{\Longleftrightarrow}} \quad H(j\omega) = \frac{1}{RC}\frac{1}{\frac{1}{RC} + j\omega} = \frac{1}{1 + j\omega RC}$$

$$|H(j\omega)| = \left|\frac{1}{1 + j\omega RC}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}} \qquad |H(-j\omega)| = |H(j\omega)| \quad \text{(even)}$$

$$\phi(\omega) = \angle H(j\omega) = -arctan\left(\frac{\omega RC}{1}\right) \qquad \phi(-\omega) = -\phi(\omega) \quad \text{(odd)}$$

- For a complex exponential input, we know

$$\begin{aligned} y(t) &= \mathcal{F}^{-1}\{H(j\omega)\cdot\pi\delta(\omega-\omega_0)\} \\ &= \mathcal{F}^{-1}\left\{|H(j\omega_0)|e^{j\phi(\omega_0)}\cdot\pi\delta(\omega-\omega_0)\right\} \\ &= |H(j\omega_0)|e^{j\phi(\omega_0)}e^{j\omega_0 t} \\ &= |H(j\omega_0)|e^{j[\omega_0 t+\phi(\omega_0)]} \end{aligned}$$

- How about plain vanilla sine and cosine functions? This is easy to figure out, since they are just combinations of two complex exponentials

$$x(t) = \cos(\omega_0 t) = \frac{1}{2}\left(e^{j\omega_0 \mathrm{t}} + e^{-j\omega_0 \mathrm{t}}\right)$$

$$y(t) = \frac{1}{2}|H(j\omega_0)|e^{j[\omega_0 t+\phi(\omega_0)]} + \frac{1}{2}|H(-j\omega_0)|e^{j[-\omega_0 t+\phi(-\omega_0)]}$$

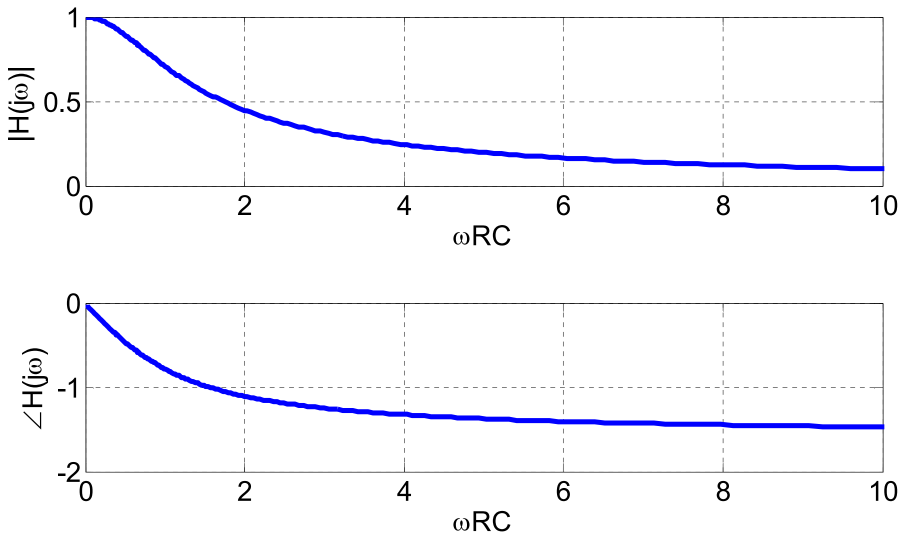
$$y(t) = \frac{1}{2}|H(j\omega_0)|e^{j[\omega_0 t+\phi(\omega_0)]} + \frac{1}{2}|H(j\omega_0)|e^{j[-(\omega_0 t+\phi(\omega_0)]}$$

$$y(t) = |H(j\omega_0)|\cos[\omega_0 t+\phi(\omega_0)]$$

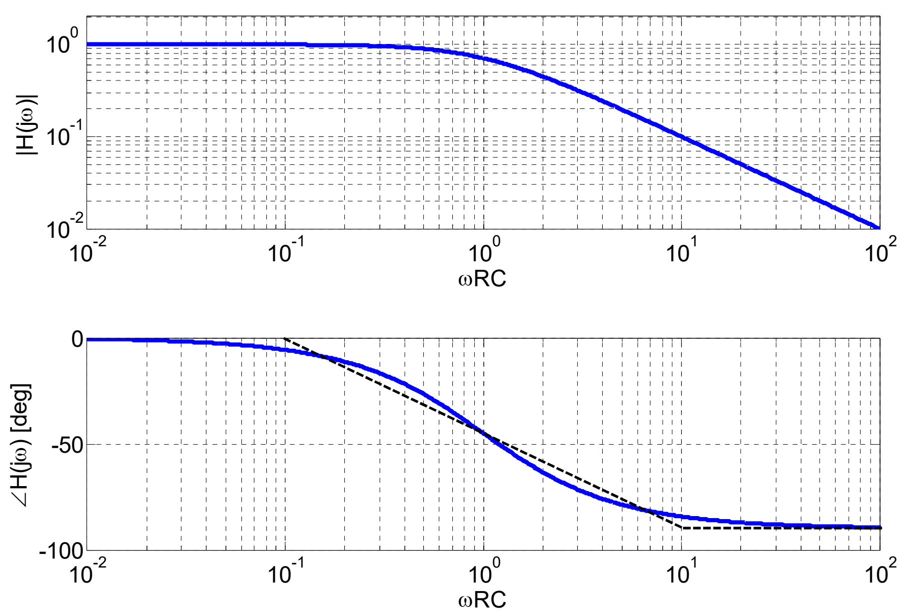
Bottom Line

- Whichever sinusoidal signal we apply, all we need to do in order to find the time domain output is
  - Scale the amplitude by the magnitude of the transfer function
  - Shift the argument by the angle of the transfer function
- Consequently, all that we'll bother to look at in detail is $H(j\omega)$
  - A circuit designer will rarely think about the actual Fourier transform of sinusoids in terms of their mathematical representations (delta functions on the positive and negative side of the ω axis)
- In addition, a circuit designer will usually not bother to draw two-sided spectra or two-sided representations of the frequency response
  - One side tells the whole story, due to known symmetries (the symmetries noted in our example hold in general)

Plotting H(jω)



Better: Magnitude log-log, angle semilog in degrees



- We can now "see" interesting breakpoints and asymptotes

Points and Slopes of Interest

$$|H(j\omega)|_{\omega=\frac{1}{RC}} = \left|\frac{1}{1+1j}\right| = \frac{1}{\sqrt{2}}$$

"Corner frequency"

$$|H(j\omega)|_{\omega\gg\frac{1}{RC}} \cong \left|\frac{1}{j\omega RC}\right| = \frac{1}{\omega RC}$$

High frequency asymptote, 10x drop per decade

$$\angle H(j\omega)_{\omega=\frac{1}{RC}} = -arctan(1) = -45°$$

Phase shift at corner frequency

$$\angle H(j\omega)_{\omega\gg\frac{1}{RC}} \cong -90°$$

Phase shift asymptote at high frequencies

The transition from small phase shift to nearly 90 degree phase shift occurs within about two frequency decades.

Magnitude in decibels (dB)

- A logarithmic unit with lots of history
  - See http://en.wikipedia.org/wiki/Decibel
- The decibel is used to express the logarithmic ratio between two quantities. The base definition is for ratios of power.

$$R_{dB} = 10\log_{10}\left(\frac{P_1}{P_0}\right) \qquad R_{dB} = 10\log_{10}\left(\frac{1W}{1\mu W}\right) = 60dB$$

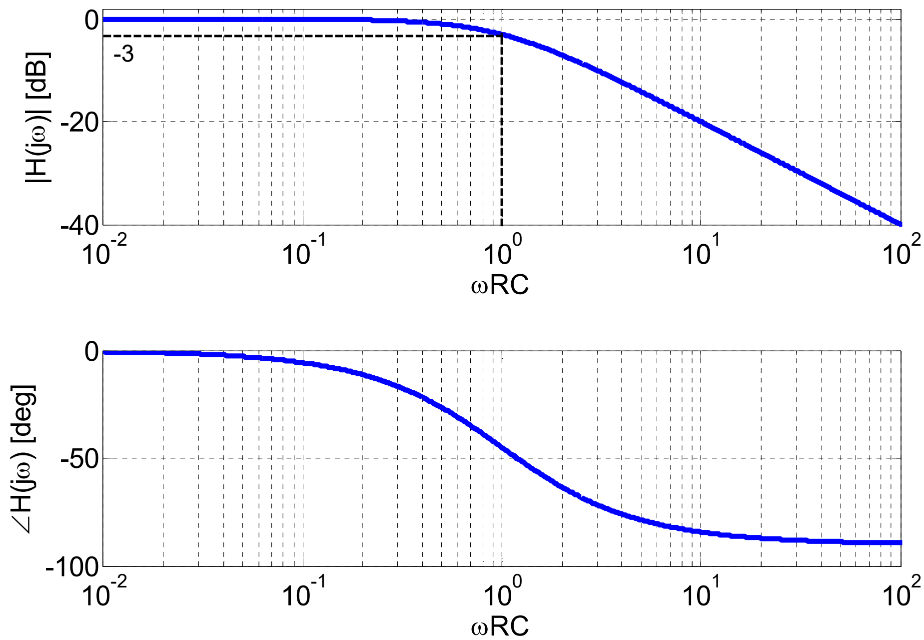
- Since power is proportional to voltage (or current) squared, we have

$$R_{dB} = 10\log_{10}\left(\frac{V_1^2}{V_0^2}\right) = 20\log_{10}\left(\frac{V_1}{V_0}\right) \qquad R_{dB} = 20\log_{10}\left(\frac{1V}{1mV}\right) = 60dB$$

- Note that

$$20\log_{10}\left(\frac{1}{\sqrt{2}}\right) = -3.0103dB \cong -3dB$$

“Bode Plot” (Magnitude in dB)



Chapter 7

The Laplace Transform

Boris Murmann

Stanford University

Reading: Smith, Chapter 32 (available on course web under “Reading Material”)
Reference: Oppenheim and Willsky, Chapter 9

Jean Baptiste Joseph Fourier
Mathematician and Physicist
1768 – 1830

Pierre-Simon Laplace
Mathematician and Astronomer
1749 – 1827

Limitations of the Fourier Transform

- The Fourier transform is a great tool for describing **signals**
- However, when it comes to describing and analyzing **systems**, the Fourier transform has a few shortcomings
  - It does not handle initial conditions
  - It does not converge/exist for certain functions of interest
  - It does not lead to a compact representation of system properties
    - Poles, zeros, more later…
- The solution to this problem is the Laplace transform, which can be viewed as a generalization of the Fourier transform
  - Often just advertised as a tool for solving differential equations
    - But, it is much more than that for electrical engineers

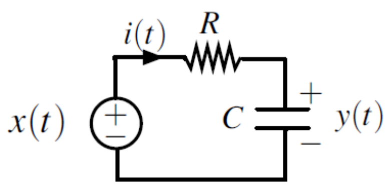
$$\text{Laplace Transform} \xrightarrow{z = e^{sT}} \text{z Transform}$$

$$\text{Laplace Transform} \xrightarrow{s = j\omega} \text{Fourier Transform}$$

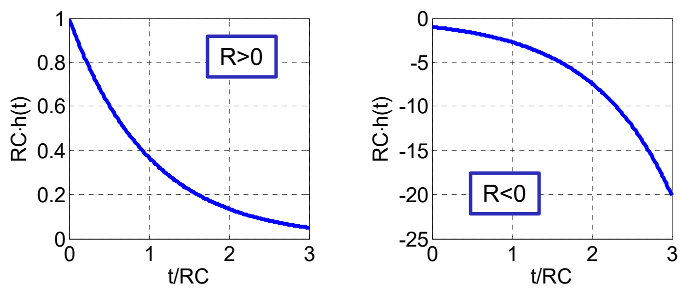
Phasor Transform

Motivating Example

- Same as analyzed in the previous chapter, but let's also consider negative values for R
  - May look strange at first glance, but we can easily build negative R with active components (and this is used in oscillators, etc.)



$$h(t) = \frac{1}{RC} e^{-\frac{t}{RC}}$$



"blows up"

Fourier Transforms

$$h(t) = e^{-at} \qquad a \geq 0 \qquad H(j\omega) = \int_{-\infty}^{\infty} e^{-at}u(t) \cdot e^{-j\omega t}\, dt = \frac{1}{a + j\omega}$$

$$h(t) = e^{bt} \qquad b \geq 0 \qquad H(j\omega) = \int_{-\infty}^{\infty} e^{bt}u(t) \cdot e^{-j\omega t} dt$$

Integral does not converge

(Bilateral) Laplace Transform

$$X(\sigma, \omega) = \int_{-\infty}^{\infty} [x(t) \cdot e^{-\sigma t}] e^{-j\omega t} dt$$

- This is really just the Fourier transform of $[x(t) \cdot e^{-\sigma t}]$
- More commonly written as

$$X(s) = \int_{-\infty}^{\infty} x(t) e^{-st} dt \qquad\qquad s = \sigma + j\omega$$

- This integral converges for a much larger class of functions that we are interested in
- Let's have a look at our specific example

Laplace Transforms

$$h(t) = e^{-at} \qquad a \geq 0 \qquad H(s) = \int_{-\infty}^{\infty} e^{-at} u(t) \cdot e^{-\sigma t} e^{-j\omega t} dt = \frac{1}{a+s}$$

Converges for $\sigma > -a$

$$h(t) = e^{bt} \qquad b \geq 0 \qquad H(s) = \int_{-\infty}^{\infty} e^{bt} u(t) \cdot e^{-\sigma t} e^{-j\omega t} dt = \frac{1}{a+s}$$

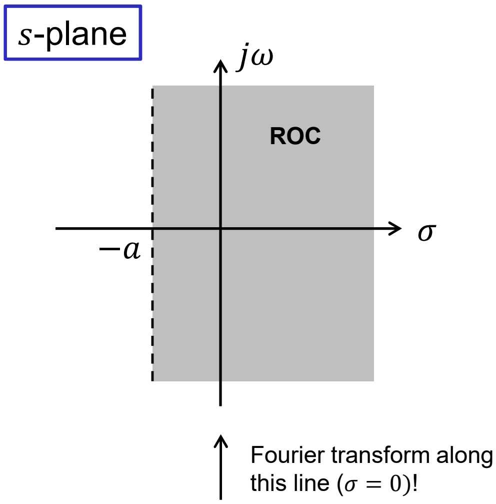
Converges for $\sigma > b$

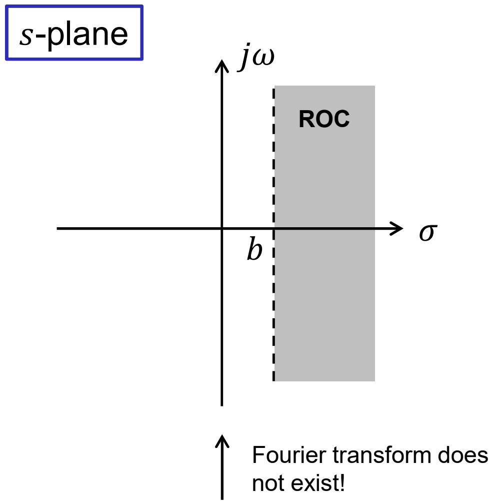
- A Laplace transform always comes with a "region of convergence" (ROC)
  - Covered in great detail in EE102B; we'll just look at this briefly

Region of Convergence

$h(t) = e^{-at} \qquad a \geq 0$

$h(t) = e^{bt} \qquad b \geq 0$





(Unilateral) Laplace Transform

$$X(s) = \int_{0-}^{\infty} x(t)e^{-st}dt$$

- The unilateral version of the Laplace transform is most commonly used in circuit texts, as it lets us deal with initial conditions
- Setting the lower integration limit to 0- makes it clear that we are including impulses (δ(t)) around t=0
- If $x(t) = 0$ for $t < 0$, the Fourier transform still follows from the unilateral Laplace transform by substituting $s = j\omega$ (just like in the more general bilateral case)
  - In the context of transforming the impulse response of a system, this is just requiring that the system is causal
- Unless otherwise noted, we will assume that Laplace transforms in EE101B are unilateral

- Note that just like $e^{j\omega t}$, e^{st} is also an eigenfunction of LTI systems

- If we have a convolution system with an impulse response $h(t)$, and and input e^{st} where $s = \sigma + j\omega$

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h(\tau) e^{s(t-\tau)}\, d\tau \\ &= e^{st} \int_{-\infty}^{\infty} h(\tau) e^{-s\tau}\, d\tau \end{aligned}$$

- We get the complex exponential back, with a complex constant multiplier

$$\begin{aligned} H(s) &= \int_{-\infty}^{\infty} h(\tau) e^{-s\tau}\, d\tau \\ y(t) &= e^{st} H(s) \end{aligned}$$

provided the integral converges.

[Pauly, EE102A]

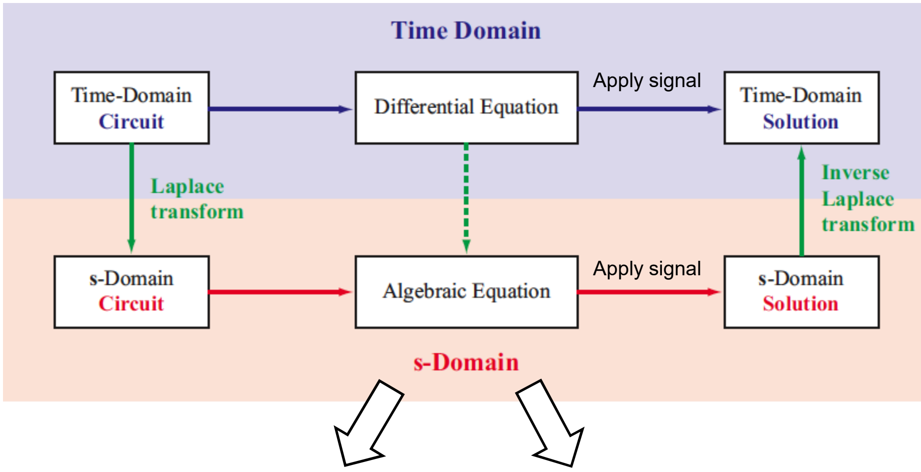
- $H(s)$ is the Laplace transform of the LTI system's impulse response, and is also called the system transfer function
- We can compute the system output using

$$Y(s) = H(s) \cdot X(s)$$

- As before (with the Fourier transform), this saves us from evaluating convolution integrals
- If the ROC of $H(s)$ includes the imaginary axis, then for $s = j\omega$, H(s) gives us the Fourier transform (frequency response) of the system

Laplace Domain Framework

[Modified from Ulaby & Maharbiz]



Gain important insight from s-domain representation (poles, zeros)

Get the frequency response (Fourier transform) by setting $s = j\omega$

	$f(t)$		$\mathbf{F}(s) = \mathcal{L}[f(t)]$
1	$\delta(t)$	⟷	1
1a	$\delta(t-T)$	⟷	e^{-Ts}
2	1 or $u(t)$	⟷	$\frac{1}{s}$
2a	$u(t-T)$	⟷	$\frac{e^{-Ts}}{s}$
3	$e^{-at}\,u(t)$	⟷	$\frac{1}{s+a}$
3a	$e^{-a(t-T)}\,u(t-T)$	⟷	$\frac{e^{-Ts}}{s+a}$
4	$t\,u(t)$	⟷	$\frac{1}{s^2}$
4a	$(t-T)\,u(t-T)$	⟷	$\frac{e^{-Ts}}{s^2}$
5	$t^2\,u(t)$	⟷	$\frac{2}{s^3}$
6	$te^{-at}\,u(t)$	⟷	$\frac{1}{(s+a)^2}$
7	$t^2e^{-at}\,u(t)$	⟷	$\frac{2}{(s+a)^3}$
8	$t^{n-1}e^{-at}\,u(t)$	⟷	$\frac{(n-1)!}{(s+a)^n}$
9	$\sin\omega t\,u(t)$	⟷	$\frac{\omega}{s^2+\omega^2}$
10	$\sin(\omega t+\theta)\,u(t)$	⟷	$\frac{s\sin\theta+\omega\cos\theta}{s^2+\omega^2}$
11	$\cos\omega t\,u(t)$	⟷	$\frac{s}{s^2+\omega^2}$
12	$\cos(\omega t+\theta)\,u(t)$	⟷	$\frac{s\cos\theta-\omega\sin\theta}{s^2+\omega^2}$
13	$e^{-at}\sin\omega t\,u(t)$	⟷	$\frac{\omega}{(s+a)^2+\omega^2}$
14	$e^{-at}\cos\omega t\,u(t)$	⟷	$\frac{s+a}{(s+a)^2+\omega^2}$
15	$2e^{-at}\cos(bt-\theta)\,u(t)$	⟷	$\frac{e^{j\theta}}{s+a+jb}+\frac{e^{-j\theta}}{s+a-jb}$
16	$\frac{2t^{n-1}}{(n-1)!}e^{-at}\cos(bt-\theta)\,u(t)$	⟷	$\frac{e^{j\theta}}{(s+a+jb)^n}+\frac{e^{-j\theta}}{(s+a-jb)^n}$

Laplace transform pairs

[Ulaby & Maharbiz]

Another common pair:

$$\frac{1}{a}(1-e^{-at})u(t) \Longleftrightarrow \frac{1}{s(s+a)}$$

(follows from 2 and 3)

Table 6-3: Properties of the Laplace transform ($f(t) = 0$ for $t < 0^-$).

Property	$f(t)$		$\mathbf{F}(\mathbf{s}) = \mathcal{L}[f(t)]$
1. Multiplication by constant	$K\ f(t)$	↔	$K\ \mathbf{F}(\mathbf{s})$
2. Linearity	$K_1\ f_1(t) + K_2\ f_2(t)$	↔	$K_1\ \mathbf{F}_1(\mathbf{s}) + K_2\ \mathbf{F}_2(\mathbf{s})$
3. Time scaling	$f(at), \quad a > 0$	↔	$\frac{1}{a}\ \mathbf{F}\left(\frac{\mathbf{s}}{a}\right)$
4. Time shift	$f(t-T)\ u(t-T)$	↔	$e^{-T\mathbf{s}}\ \mathbf{F}(\mathbf{s}), \quad T \geq 0$
5. Frequency shift	$e^{-at}\ f(t)$	↔	$\mathbf{F}(\mathbf{s}+a)$
6. Time 1st derivative	$f' = \frac{df}{dt}$	↔	$\mathbf{s}\ \mathbf{F}(\mathbf{s}) - f(0^-)$
7. Time 2nd derivative	$f'' = \frac{d^2 f}{dt^2}$	↔	$\mathbf{s}^2\mathbf{F}(\mathbf{s}) - \mathbf{s} f(0^-) - f'(0^-)$
8. Time integral	$\int_{0^-}^{t} f(t')\ dt'$	↔	$\frac{1}{\mathbf{s}}\ \mathbf{F}(\mathbf{s})$
9. Frequency derivative	$t\ f(t)$	↔	$-\frac{d}{d\mathbf{s}}\ \mathbf{F}(\mathbf{s})$
10. Frequency integral	$\frac{f(t)}{t}$	↔	$\int_{\mathbf{s}}^{\infty} \mathbf{F}(\mathbf{s}')\ d\mathbf{s}'$

[Ulaby & Maharbiz]

Derivative ↔ Multiplication with *s*

Integral ↔ Division by *s*

Proof of Derivative Property

If we write the definition of $\mathcal{L}(f'(t))$, we get

$$\mathcal{L}(f'(t)) = \int_0^{+\infty} f'(t) e^{-st} dt.$$

If we set $u'(t) = f'(t)$ and $v(t) = e^{-st}$, from the integration by parts formula, we get

$$\mathcal{L}(f'(t)) = \left[f(t)e^{-st}\right]_{t=0}^{+\infty} - \int_0^{+\infty} f(t)\,(-s)\,e^{-st} dt$$
$$= \left[f(t)e^{-st}\right]_{t=0}^{+\infty} + s\int_0^{+\infty} f(t)e^{-st} dt.$$

If we assume that, as t goes to $+\infty$, $f(t)e^{-st} \to 0$, then:

$$\mathcal{L}(f'(t)) = 0 - f(0) + s\int_0^{+\infty} f(t)e^{-st} dt = s\mathcal{L}(f(t)) - f(0).$$

[Darve, CME102]

Laplace Transform of Circuits/Circuit Elements

- One way to use the Laplace transform is to write the differential equation, translate into an algebraic equation and then solve
  - Circuit designers are far too lazy to do this…
- What we'll do is apply the Laplace transform to each component and write KCL/KVL in the Laplace domain

KCL $\mathcal{L}\left(\sum i_j(t)=0\right)$ $\sum \mathcal{L}\{i_j(t)\}=0$ $\sum I_j(s)=0$

KVL $\mathcal{L}\left(\sum v_j(t)=0\right)$ $\sum \mathcal{L}\{v_j(t)\}=0$ $\sum V_j(s)=0$

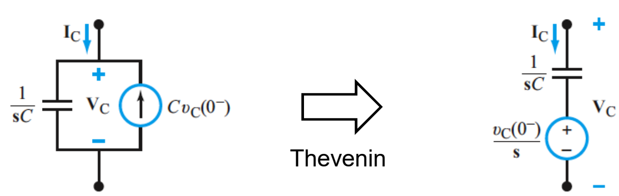
Resistor $\mathcal{L}\{v(t)=Ri(t)\}$ $\mathcal{L}\{v(t)\}=R\cdot\mathcal{L}\{i(t)\}$ $V(s)=R\cdot I(s)$

Capacitor

$$i_C(t)=C\frac{dv_C(t)}{dt}$$

$$\mathcal{L}\{i_C(t)\}=C\cdot\mathcal{L}\left\{\frac{dv_C(t)}{dt}\right\}$$

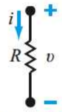
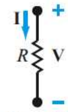
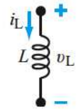
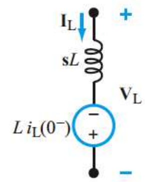
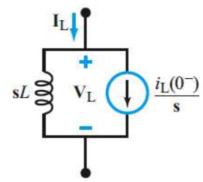
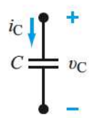
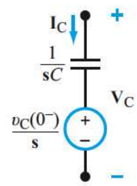
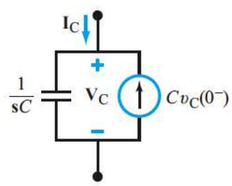
$$I_C(s)=sC\cdot V_C(s)-Cv_C(0^-)$$



- If $v_C(0^-)=0$, we can define s-domain impedances and admittances, similar to (resistance and conductance for a resistor)

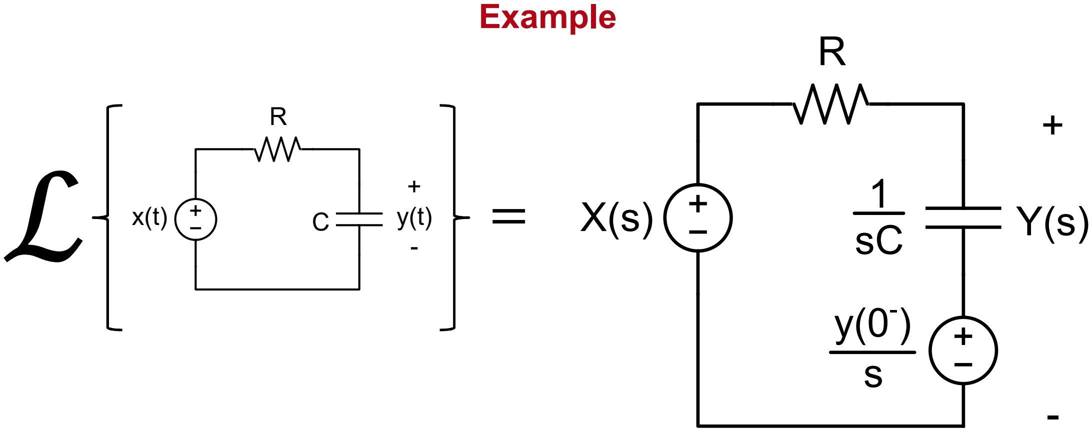
$$I_C(s)=sC\cdot V_C(s) \qquad Z_C(s)=\frac{V_C(s)}{I_C(s)}=\frac{1}{sC} \qquad Y_C(s)=\frac{1}{Z(s)}=sC$$

Table 6-6: Circuit models for R, L, and C in the s-domain.

Time-Domain	s-Domain		
Resistor  $\upsilon = Ri$	 $\mathbf{V} = R\mathbf{I}$		
Inductor  $\upsilon_L = L\dfrac{di_L}{dt}$ $i_L = \dfrac{1}{L}\displaystyle\int_{0^-}^{t} \upsilon_L\,dt + i_L(0^-)$	 $\mathbf{V}_L = \mathbf{s}L\mathbf{I}_L - L\,i_L(0^-)$	OR	 $\mathbf{I}_L = \dfrac{\mathbf{V}_L}{\mathbf{s}L} + \dfrac{i_L(0^-)}{\mathbf{s}}$
Capacitor  $i_C = C\dfrac{d\upsilon_C}{dt}$ $\upsilon_C = \dfrac{1}{C}\displaystyle\int_{0^-}^{t} i_C\,dt + \upsilon_C(0^-)$	 $\mathbf{V}_C = \dfrac{\mathbf{I}_C}{\mathbf{s}C} + \dfrac{\upsilon_C(0^-)}{\mathbf{s}}$	OR	 $\mathbf{I}_C = \mathbf{s}C\mathbf{V}_C - C\,\upsilon_C(0^-)$

[Ulaby & Maharbiz]

Example



$$Y(s) = X(s)\frac{\frac{1}{sC}}{R+\frac{1}{sC}} + \frac{y(0^-)}{s}\cdot\frac{R}{R+\frac{1}{sC}} = [X(s) + RCy(0^-)]\frac{1}{1+sRC}$$

If $y(0^-) = 0$: $$H(s) = \frac{Y(s)}{X(s)} = \frac{1}{1+sRC}$$

Chapter 8

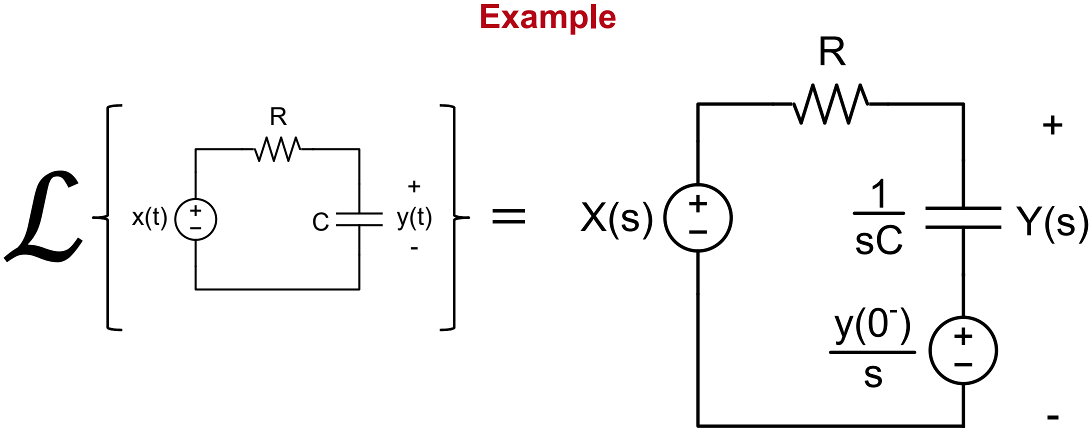
Analysis of First Order Circuits Using the Laplace Transform

Boris Murmann

Stanford University

Reading: Smith, Chapter 32 (available on course web under “Reading Material”)
Reference: Oppenheim and Willsky, Chapter 9

Example



$$Y(s) = X(s)\frac{\frac{1}{sC}}{R+\frac{1}{sC}} + \frac{y(0^-)}{s}\cdot\frac{R}{R+\frac{1}{sC}} = [X(s) + RCy(0^-)]\frac{1}{1+sRC}$$

If $y(0^-) = 0$: $$H(s) = \frac{Y(s)}{X(s)} = \frac{1}{1+sRC}$$

Let's Compute…

- The impulse response
- The pole location of the circuit
- The frequency response
- The zero input response with an initial condition
- The step response
- The response to a stepped cosine

Impulse Response

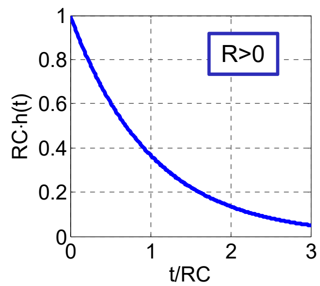
- Set initial condition to zero
- Look up Laplace transform of $\delta(t)$ in the transform pair table

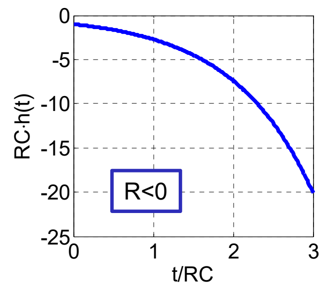
$$H(s) = \frac{1}{1 + sRC} \qquad X(s) = \mathcal{L}\{\delta(t)\} = 1$$

$$Y(s) = H(s)X(s) = \frac{1}{1 + sRC} \cdot 1 = H(s)$$

$$\frac{1}{s+a} \leftrightarrow e^{-at} \qquad h(t) = \frac{1}{RC} e^{-\frac{t}{RC}}$$

(as we already knew…)





"blows up"

Stability

- In general, a system is said to be stable if every bounded input produces a bounded output (BIBO)
- For an LTI system, it can be shown that stability requires the impulse response to be absolutely integrable, i.e. $\int_{-\infty}^{\infty} |h(t)| dt < \infty$
  – Means that the RC circuit with R>0 is stable, the circuit with R<0 is not
- For a causal LTI system with a rational $H(s)$, this condition is equivalent to having all the "poles" of $H(s)$ in the left half of the s-plane
- The poles $(p_1 \ldots p_n)$ are the roots of the denominator polynomial of $H(s)$, the zeros $(z_1 \ldots z_n)$ are the roots of the numerator polynomial

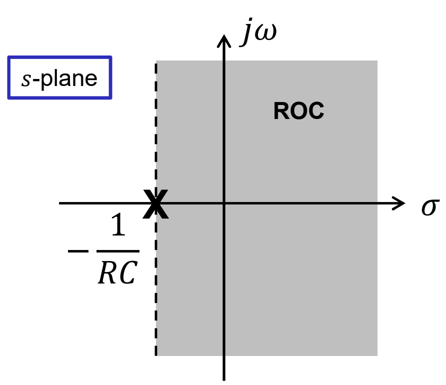
$$H(s) = \frac{N(s)}{D(s)} = \frac{a_0 + a_1 s + \cdots + a_m s^m}{b_0 + b_1 s + \cdots + b_n s^n} = K \frac{(s - z_1)(s - z_1) \ldots (s - z_n)}{(s - p_1)(s - p_2) \ldots (s - p_n)}$$

$$H(s) = G \frac{\left(1 - \frac{s}{z_1}\right)\left(1 - \frac{s}{z_2}\right) \ldots \left(1 - \frac{s}{z_m}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \ldots \left(1 - \frac{s}{p_n}\right)} \qquad G = \frac{a_0}{b_0}$$

Stability of our RC Circuit

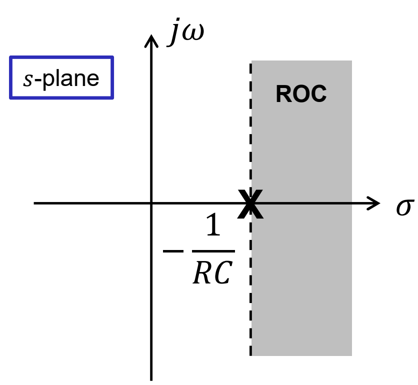
$$H(s) = \frac{1}{1 + sRC} = \frac{1}{1 - \frac{s}{p}} \qquad p = -\frac{1}{RC}$$

R > 0 → pole in the left half plane

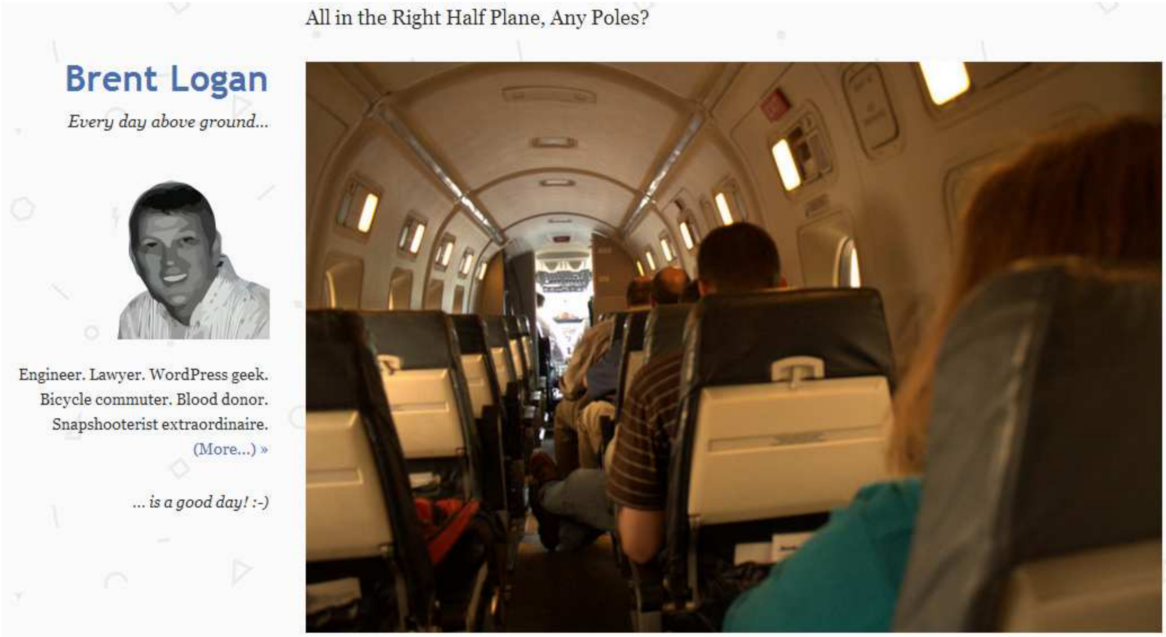


STABLE

R < 0 → pole in the right half plane

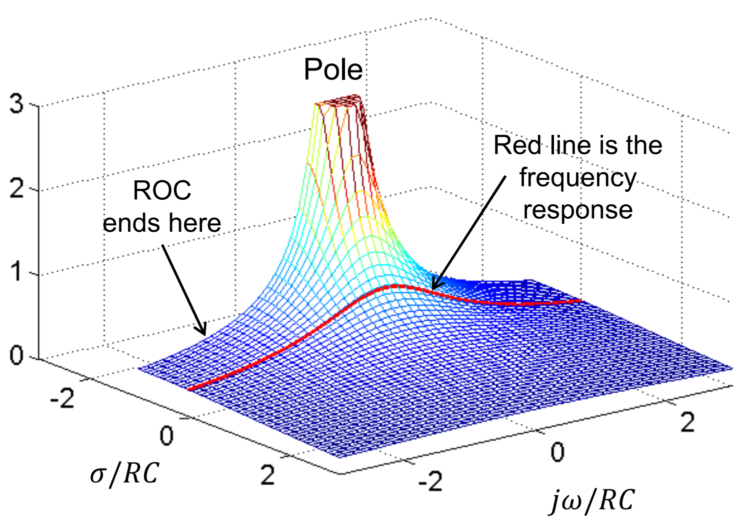


UNSTABLE

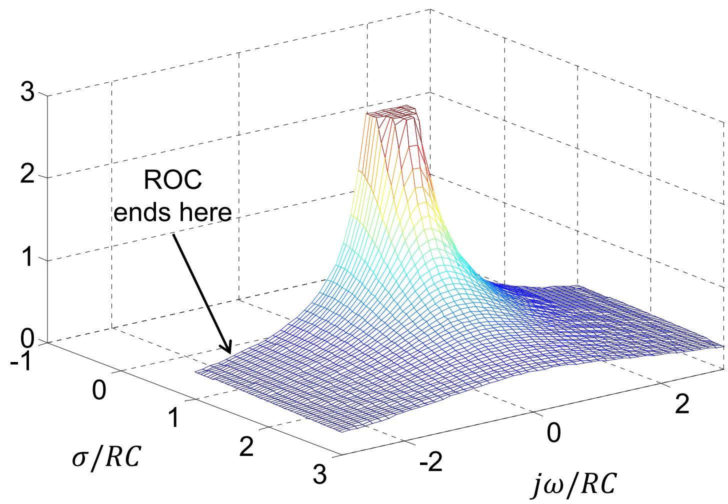


3D Plot of $|H(s)|$ for R>0

$$H(s) = \frac{1}{1 + sRC} \qquad H(\sigma, j\omega) = \left|\frac{1}{1 + (\sigma + j\omega)RC}\right|$$



3D Plot of $|H(s)|$ for R<0



- The circuit is unstable and the frequency response is undefined (the $j\omega$ axis lies outside the ROC)

Frequency Response

- If the circuit is stable, the frequency response is simply found by evaluating $H(s)$ for $s = j\omega$

$$H(s) = \frac{1}{1 + sRC}$$

$$H(j\omega) = H(s)\Big|_{s=j\omega} = \frac{1}{1 + j\omega RC}$$

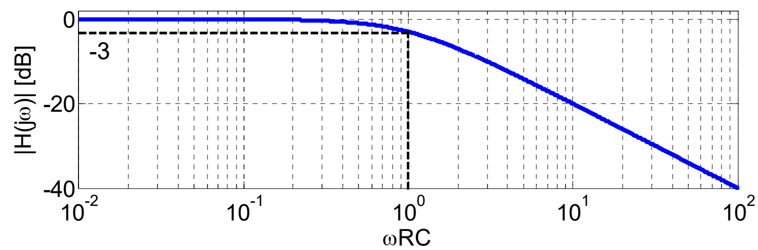
$$|H(j\omega)| = \left|\frac{1}{1 + j\omega RC}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

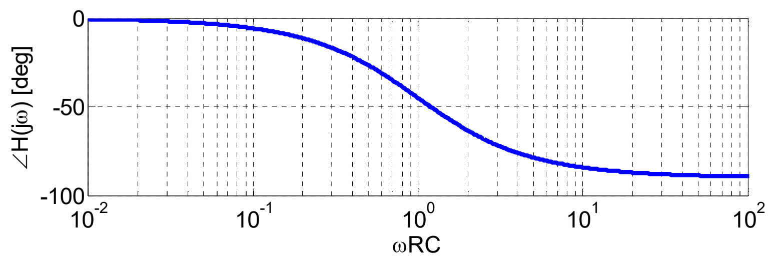
$$\angle H(j\omega) = -arctan(\omega RC)$$

Bode Plot

- The angular corner frequency coincides with the magnitude of the pole
  - This is only the case for a single pole system

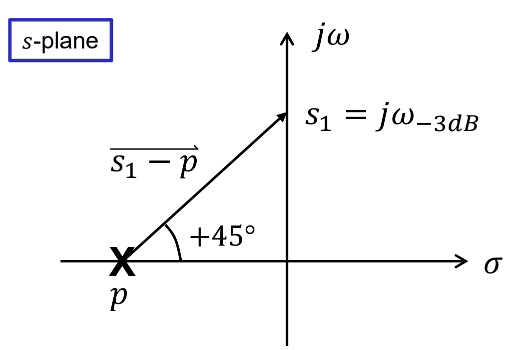
$$\omega_{-3dB} = \frac{1}{RC} = |p|$$





Geometrical Interpretation

$$H(s) = \frac{1}{1+sRC} = \frac{-p}{s-p} \qquad p = -\frac{1}{RC}$$



$$|H(s_1)| = \frac{|-p|}{|s-p|} = \frac{|p|}{|p|\sqrt{2}} = \frac{1}{\sqrt{2}}$$

$$\angle H(s_1) = -45°$$

Bode Plot Construction Rules (For Real Poles and Zeros)

$$H(s) = G\frac{\left(1-\frac{s}{z_1}\right)\left(1-\frac{s}{z_2}\right)\ldots\left(1-\frac{s}{z_m}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\ldots\left(1-\frac{s}{p_n}\right)}$$

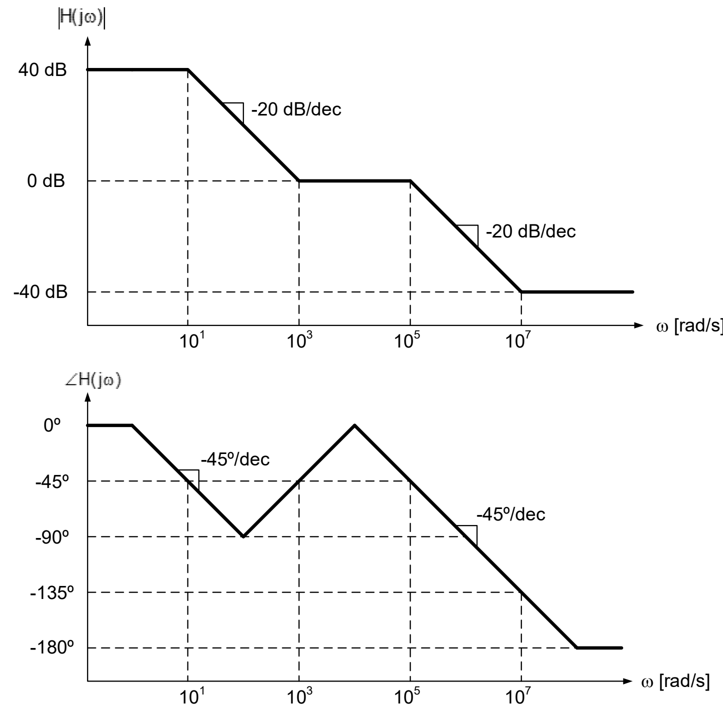
$$\log|H(j\omega)| = \log|G| + \log\left|1-\frac{j\omega}{z_1}\right| + \cdots - \log\left|1-\frac{j\omega}{p_1}\right| - \cdots$$

- Identify all the pole frequencies ω_{pi} and ω_{zi} and list them in increasing order. Apply the following rules, beginning with the lowest frequency.
- For each zero, the magnitude slope increases by 20 dB/decade, when the frequency is greater than the zero frequency.
- For each pole, the magnitude slope decreases by 20 dB/decade when the frequency is greater than the pole frequency.
- To plot the phase, we know that each term contributes +45° for a LHP zero, and – 45° for a RHP zero at ω_{zi}. A real pole contributes –45°. We approximate the total ±90° phase shift as a straight line over the interval $0.1\omega_i < \omega < 10\omega_i$.

Example

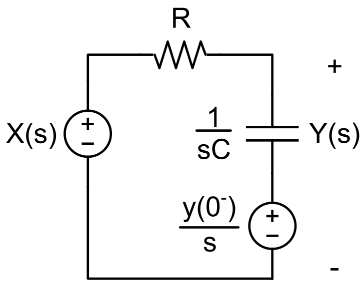
Construct a Bode plot for a system with the following parameters:

G = 100 (DC gain)
ω_{p1} = 10 rad/s
ω_{p2} = 100 krad/s
LHP zero: ω_{z1} = 1 krad/s
RHP zero: ω_{z2} = 10 Mrad/s



Computing the Zero Input Response

- Also called the natural response of the circuit



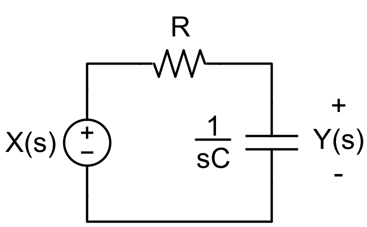
$$Y(s) = [\cancel{X(s)} + RCy(0^-)]\frac{1}{1+sRC}$$

$$Y(s) = y(0^-)\frac{1}{s+\frac{1}{RC}} \qquad \mathcal{L}^{-1}\left\{\frac{1}{s-a}\right\} = e^{at}$$

$$y(t) = y(0^-)e^{-\frac{t}{RC}}$$

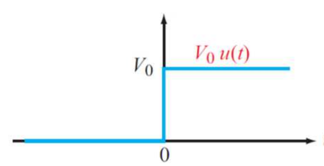
- The initial condition simply dies out exponentially
  - RC is called the time constant of the circuit, often denoted $\tau = RC$
- We got the same result by solving the differential equation
  - But this time without dealing with differential equations…

Computing the Step Response



$$x(t) = V_0 u(t)$$

$$\mathcal{L}\{u(t)\} = \frac{1}{s}$$



$$Y(s) = H(s)X(s) = \frac{1}{1+sRC}X(s) = \frac{aV_0}{s(s+a)} \qquad a = \frac{1}{RC}$$

- We could use $\mathcal{L}^{-1}\left\{\frac{1}{s(s+a)}\right\} = \frac{1}{a}(1-e^{-at})$ to solve, but let's perform a partial fraction expansion to gain some valuable insight

$$Y(s) = \frac{aV_0}{s(s+a)} = \frac{A}{s} + \frac{B}{s+a} = \frac{A(s+a)+Bs}{s(s+a)}$$

$$Y(s) = \frac{aV_0}{s(s+a)} = \frac{A}{s} + \frac{B}{s+a} = \frac{A(s+a)+Bs}{s(s+a)}$$

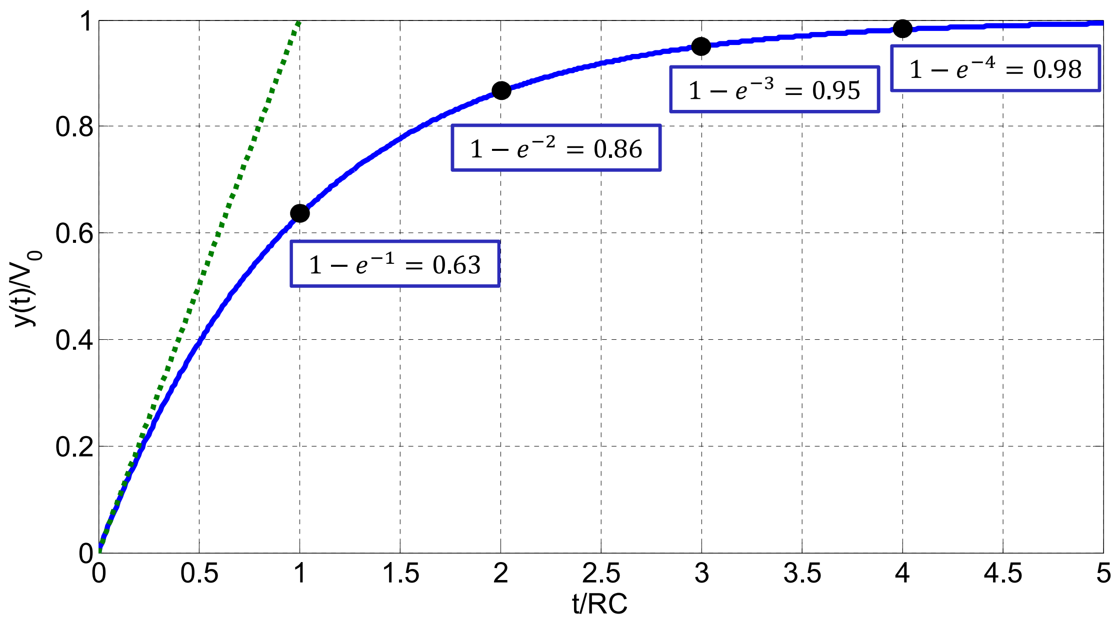
$s = 0$: $\quad aV_0 = A(s+a) \quad A = V_0 \left.\frac{a}{s+a}\right|_{s=0} = V_0 H(0)$ Transfer function at DC

$s = -a$: $\quad aV_0 = B(-a) \quad B = -V_0$

$$Y(s) = \frac{V_0 H(0)}{s} - \frac{V_0}{s+a}$$

$$y(t) = \underbrace{V_0 H(0)}_{\text{Steady-state response}} - \underbrace{V_0 e^{-\frac{t}{RC}}}_{\text{Transient response}} = V_0\left(1 - e^{-\frac{t}{RC}}\right)$$

- This result can be generalized for arbitrary $H(s) = A(s)/B(s)$
  - The steady state component, or “final value” of the step response is always $V_0 H(0)$; the transient part depends on the specifics of $H(s)$



- $\tau = RC$ is called the “settling time constant” in this context

Closely Related: The Final Value Theorem

- If $\lim_{t\to\infty} y(t)$ exists, then

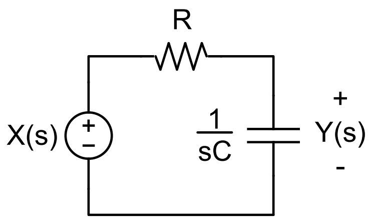
$$\lim_{t\to\infty} y(t) = \lim_{s\to 0} sY(s)$$

- For the previous example

$$\lim_{t\to\infty} y(t) = \lim_{s\to 0}\left(s \cdot \frac{aV_0}{s(s+a)}\right) = V_0$$

- This theorem is useful for arbitrary responses (not just the step response)

Computing the Response to a Stepped Cosine



$$x(t) = u(t) \cdot \cos(\omega_0 t)$$

$$\mathcal{L}\{x(t)\} = \frac{s}{s^2 + \omega_0^2} = \frac{s}{(s - j\omega_0)(s + j\omega_0)}$$

$$Y(s) = X(s)\frac{1}{1 + sRC} = \frac{as}{(s - j\omega_0)(s + j\omega_0)(s + a)} \qquad a = \frac{1}{RC}$$

- This expression is nowhere to be found in the transform pair table
- Must perform a partial fraction expansion

Partial Fraction Expansion

$$Y(s) = \frac{as}{(s - j\omega_0)(s + j\omega_0)(s + a)} = \frac{A}{s - j\omega_0} + \frac{A^*}{s + j\omega_0} + \frac{B}{s + a}$$

$$= \frac{A(s + j\omega_0)(s + a) + A^*(s - j\omega_0)(s + a) + B(s - j\omega_0)(s + j\omega_0)}{(s - j\omega_0)(s + j\omega_0)(s + a)}$$

$$s = j\omega_0: \qquad aj\omega_0 = A(j\omega_0 + j\omega_0)(j\omega_0 + a) \qquad A = \frac{a/2}{a + j\omega_0}$$

$$s = -a: \qquad a(-a) = B(-a - j\omega_0)(-a + j\omega_0) \qquad B = -\frac{a^2}{a^2 + \omega_0^2}$$

- Interestingly, note that

$$A = \frac{a/2}{a + j\omega_0} = \frac{1/2}{1 + j\omega_0 RC} = \frac{1}{2}H(j\omega_0) \qquad B = -\frac{1}{1 + (\omega_0 RC)^2} = -|H(j\omega_0)|^2$$

Putting It All Together

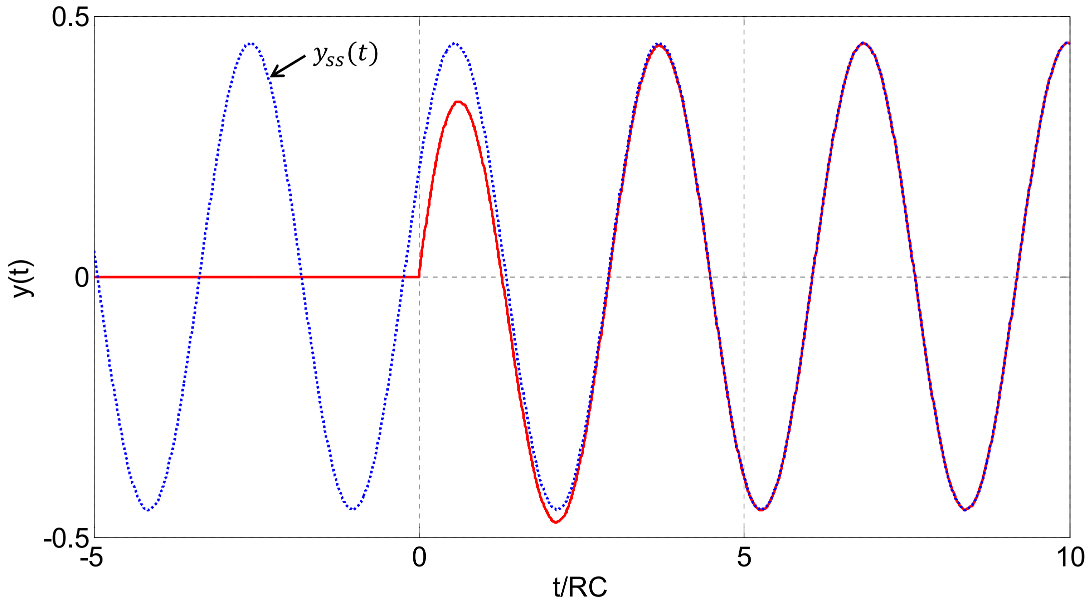
$$Y(s) = \frac{\frac{1}{2}H(j\omega_0)}{s - j\omega_0} + \frac{\frac{1}{2}H^*(j\omega_0)}{s + j\omega_0} - \frac{|H(j\omega_0)|^2}{s + a}$$

$$y(t) = \frac{1}{2}H(j\omega_0)e^{j\omega_0 t} + \frac{1}{2}H^*(j\omega_0)e^{-j\omega_0 t} - |H(j\omega_0)|^2 e^{-\frac{t}{RC}}$$

$$y(t) = \underbrace{|H(j\omega_0)|\cos[\omega_0 t + \angle H(j\omega_0)]}_{\substack{\text{Steady-state response} \\ y_{ss}(t)}} - \underbrace{|H(j\omega_0)|^2 e^{-\frac{t}{RC}}}_{\substack{\text{Transient response} \\ y_{tr}(t)}}$$

- After several time constants, the circuit approaches the steady-state response, which is the same response we obtain from the Fourier transform (or phasor transform) for everlasting sinusoids

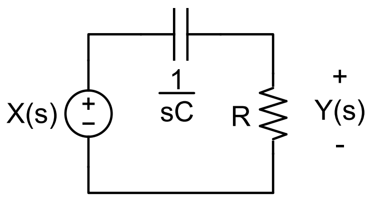
Example ($\omega_0 RC = 2$)



More Examples

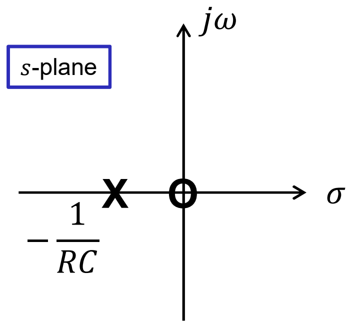
- Pole, zero and frequency response of
  - A first-order RC highpass
  - An RC lowpass with extra resistor
  - An amplifier circuit with a RHP zero
- Bode plot and asymptotes of parallel and series RC impedance

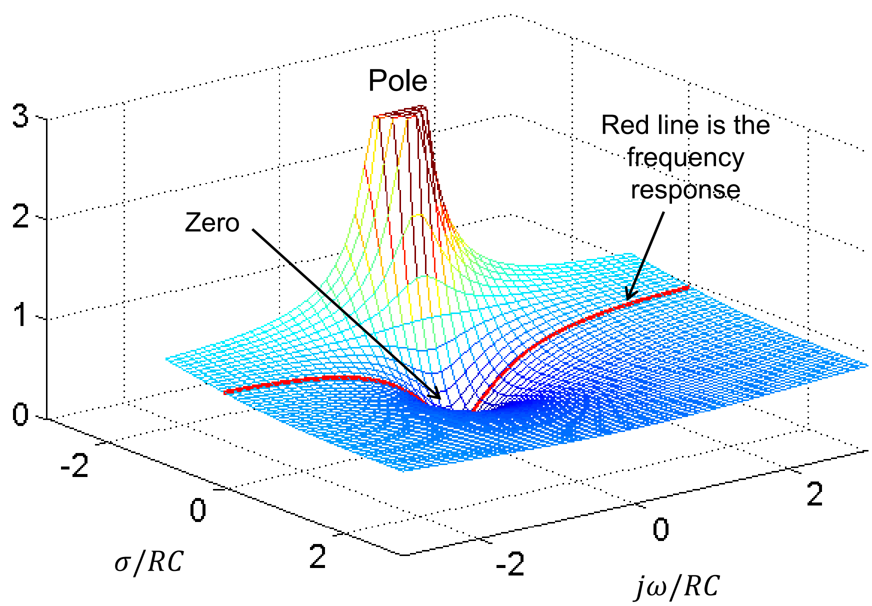
First Order RC Highpass



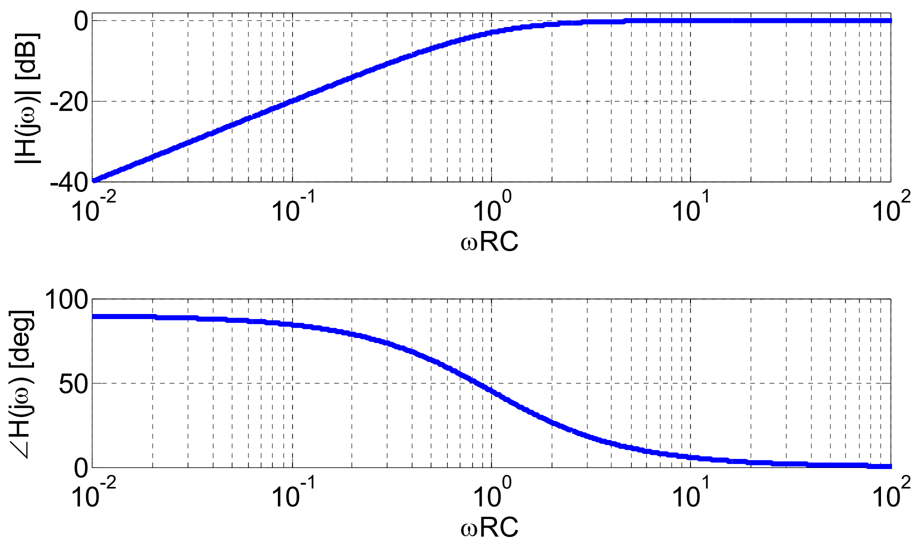
$$H(s) = \frac{Y(s)}{X(s)} = \frac{R}{R + \frac{1}{sC}} = \frac{s}{s + \frac{1}{RC}}$$

$$H(s) = \frac{s - z}{s - p} \qquad z = 0 \qquad p = -\frac{1}{RC}$$

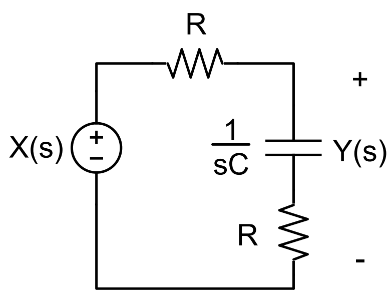




Bode Plot of the Frequency Response



RC Lowpass with Extra Resistor



$$H(s) = \frac{Y(s)}{X(s)} = \frac{R + \frac{1}{sC}}{R + \frac{1}{sC} + R} = \frac{1 + sRC}{1 + 2sRC}$$

$$H(s) = \frac{1 - \frac{s}{z}}{1 - \frac{s}{p}} \qquad z = -\frac{1}{RC} \qquad p = -\frac{1}{2RC}$$

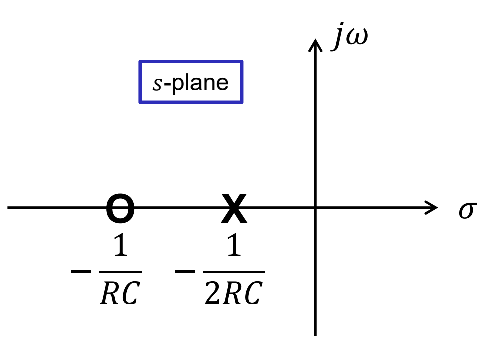
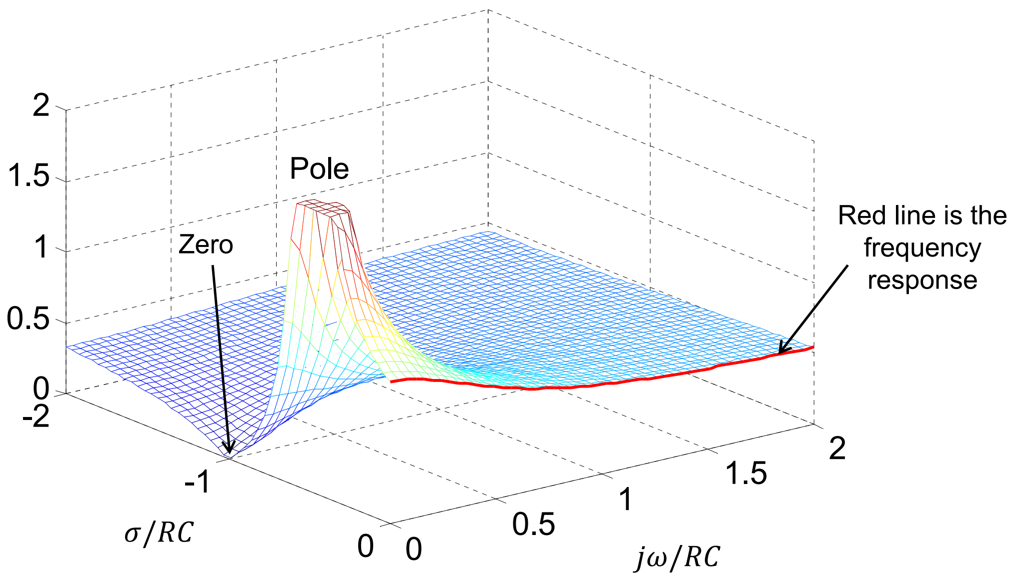
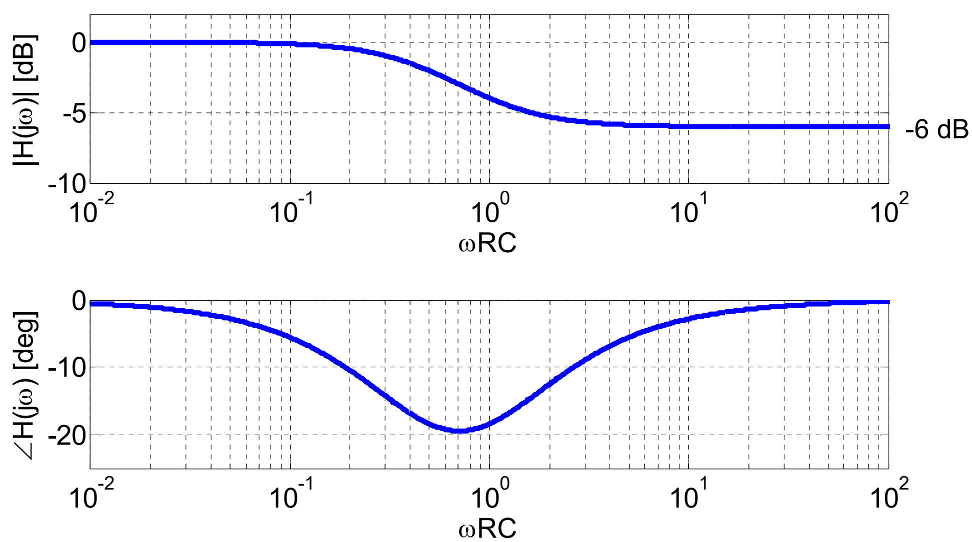


Figure 3-4



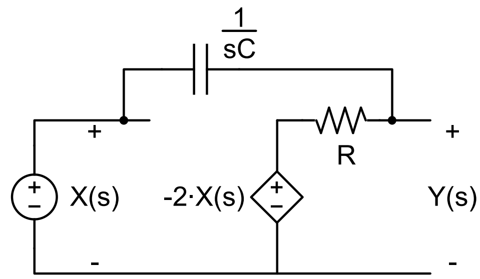
Bode Plot



- Intuition: At high frequencies, the capacitor becomes a “short” and the circuit turns into a resistive voltage divider (ratio ½, no phase shift)

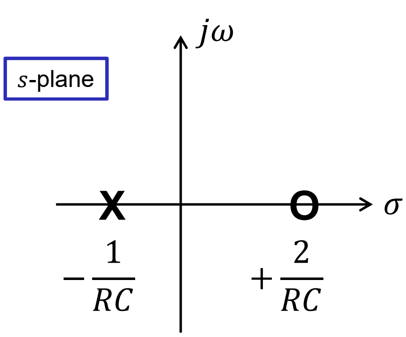
Amplifier Circuit with a RHP Zero

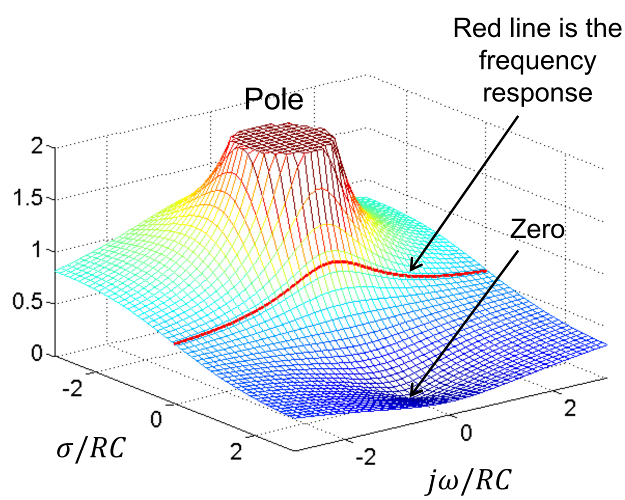
- In electronic circuits, right half plane zeros are typically caused by some sort of feedforward mechanism

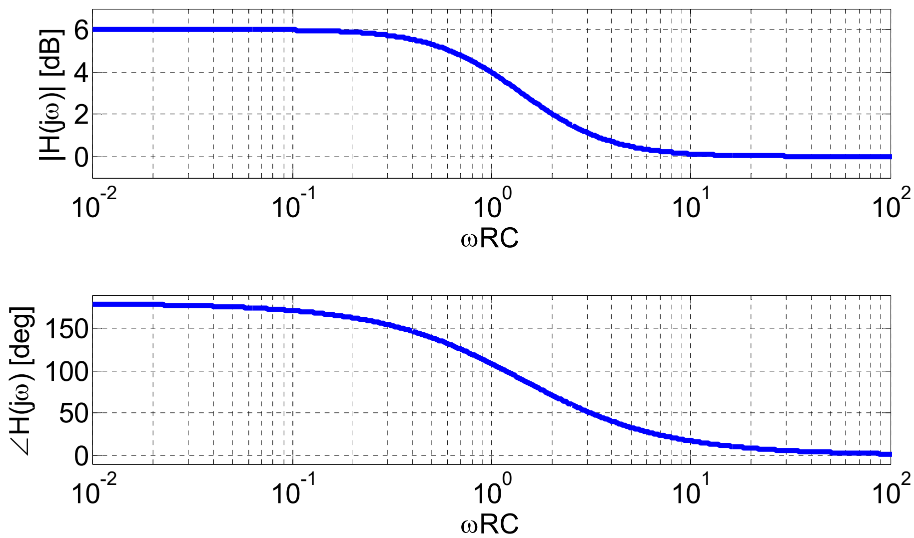


$$Y(s) = -2X(s) \cdot \frac{1}{1+sRC} + X(s)\frac{sRC}{1+sRC}$$

$$H(s) = \frac{Y(s)}{X(s)} = -2 \cdot \frac{1 - s\frac{RC}{2}}{1+sRC} \qquad z = +\frac{2}{RC} \qquad p = -\frac{1}{RC}$$

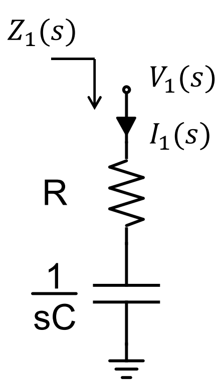


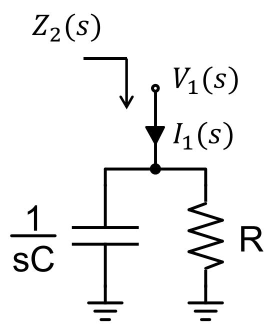




- The circuit goes through a total phase shift of -180 degrees
- At low frequencies, the amplifier is inverting with a gain of 2
- At high frequencies, the amplifier is non-inverting with unity gain

Circuit Impedances





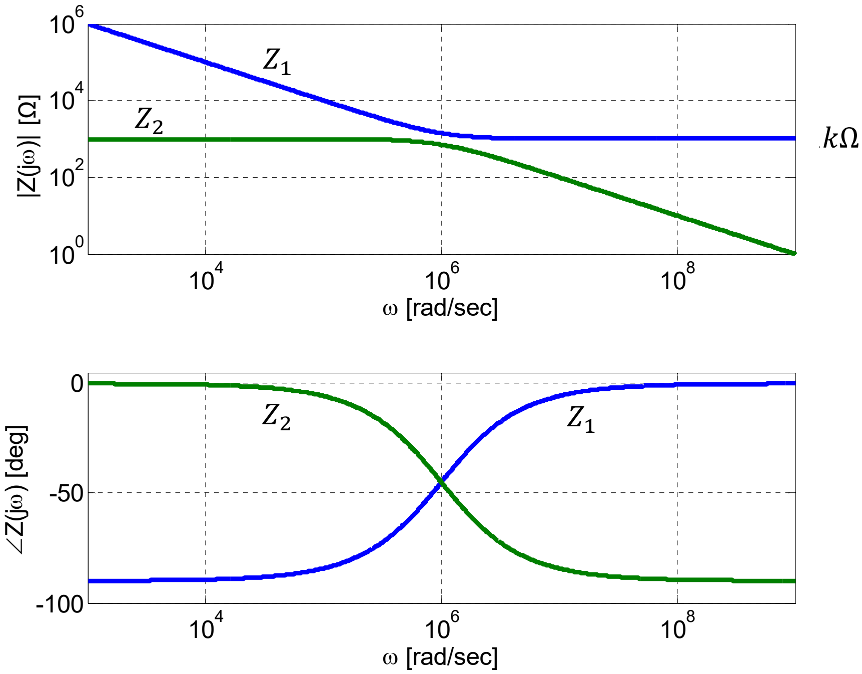
$$Z_1(s) = \frac{V_1(s)}{I_1(s)} = R + \frac{1}{sC} = \frac{1}{sC}(1 + sRC)$$

- Looks capacitive at low frequencies
- Resistive at high frequencies after going through a LHP zero

$$Z_2(s) = \frac{V_1(s)}{I_1(s)} = \left(\frac{1}{R} + sC\right)^{-1} = \frac{R}{1 + sRC}$$

- Looks resistive at low frequencies
- Capacitive at high frequencies after going through a LHP pole

Example (R = 1kΩ, C = 1nF)



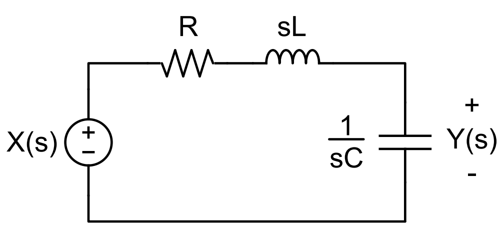
Chapter 9
Analysis of Second Order Circuits Using the Laplace Transform

Boris Murmann

Stanford University

Reading: Smith, Chapter 32 (available on course web under “Reading Material”)
Reference: Oppenheim and Willsky, Chapter 9

Second Order RLC Lowpass



$$H(s) = \frac{Y(s)}{X(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + sL + R} = \frac{1}{1 + sRC + s^2LC}$$

- A common way to parameterize this expression is

$$H(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \qquad \omega_0 = \frac{1}{\sqrt{LC}} \qquad Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

- Note that

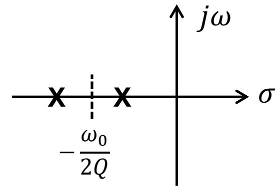
$$H(0) = 1 \qquad |H(j\omega_0)| = \left| \frac{1}{1 + \frac{j\omega_0}{\omega_0 Q} + \frac{-\omega_0^2}{\omega_0^2}} \right| = Q$$

Pole Locations

$$1+\frac{p}{\omega_0 Q}+\frac{p^2}{\omega_0^2}=0$$

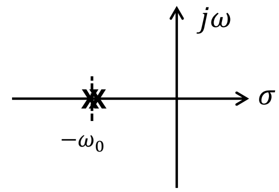
For $Q < 0.5$: $\quad p_{1,2} = -\frac{\omega_0}{2Q}\left(1 \pm \sqrt{1-4Q^2}\right)$

→ Distinct real poles



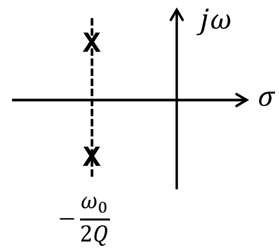
For $Q = 0.5$: $\quad p_{1,2} = -\omega_0$

→ Coincident real poles

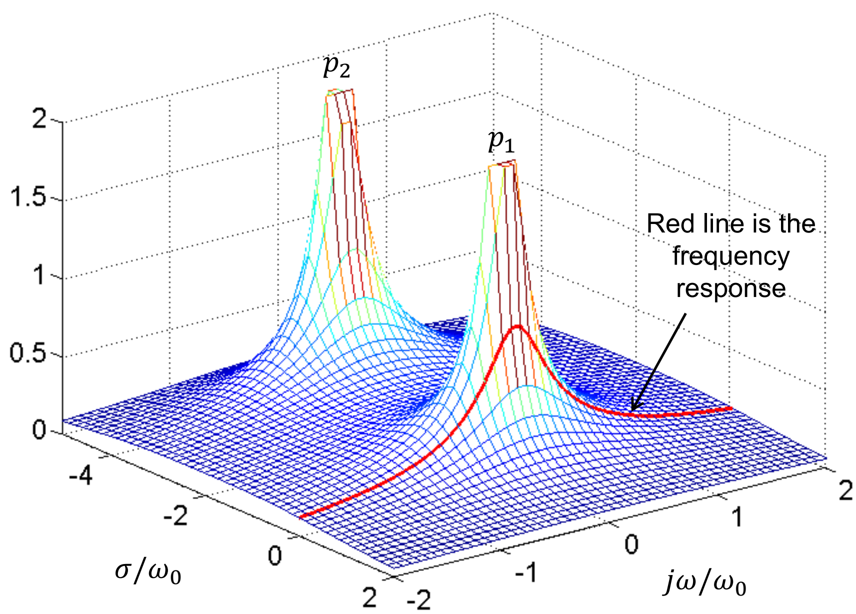


For $Q > 0.5$: $\quad p_{1,2} = -\frac{\omega_0}{2Q}\left(1 \pm j\sqrt{4Q^2-1}\right)$

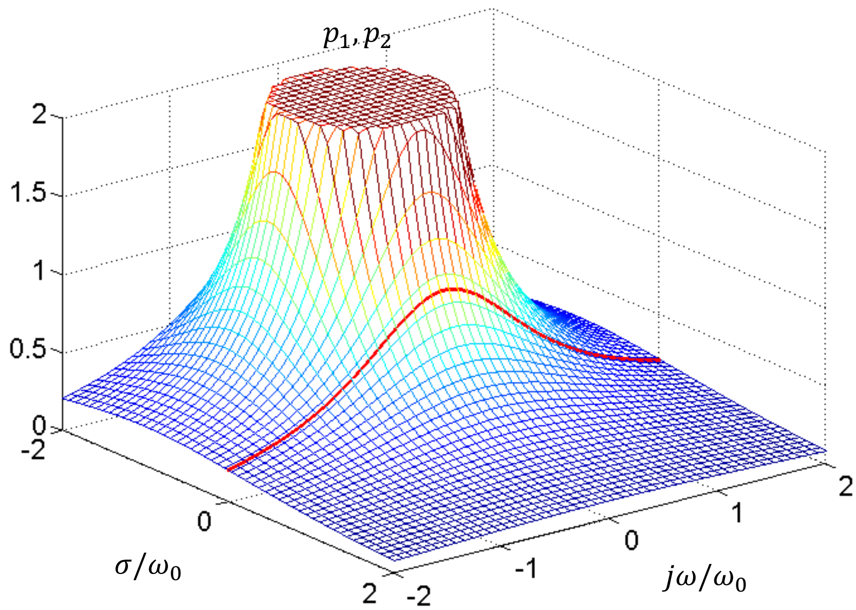
→ Complex conjugate poles



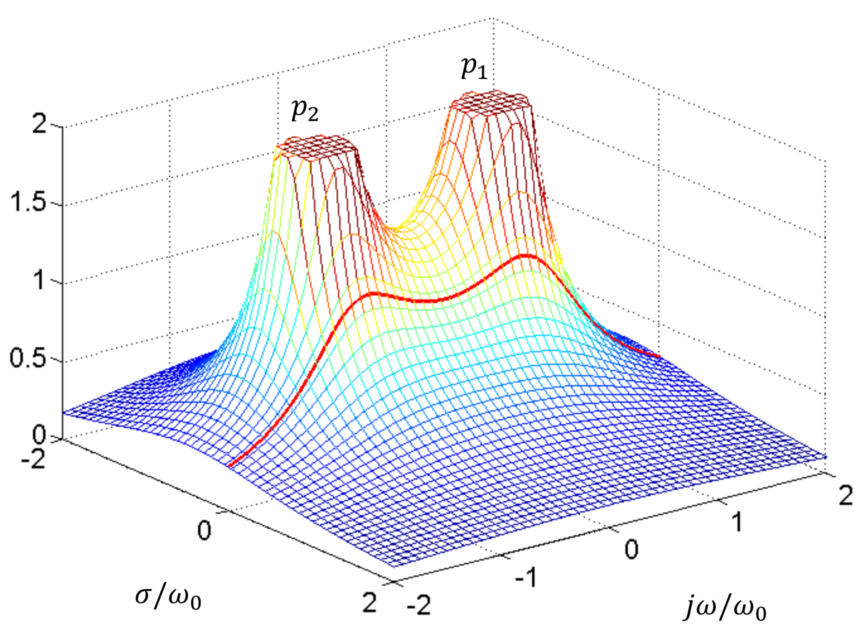
Q = 0.25



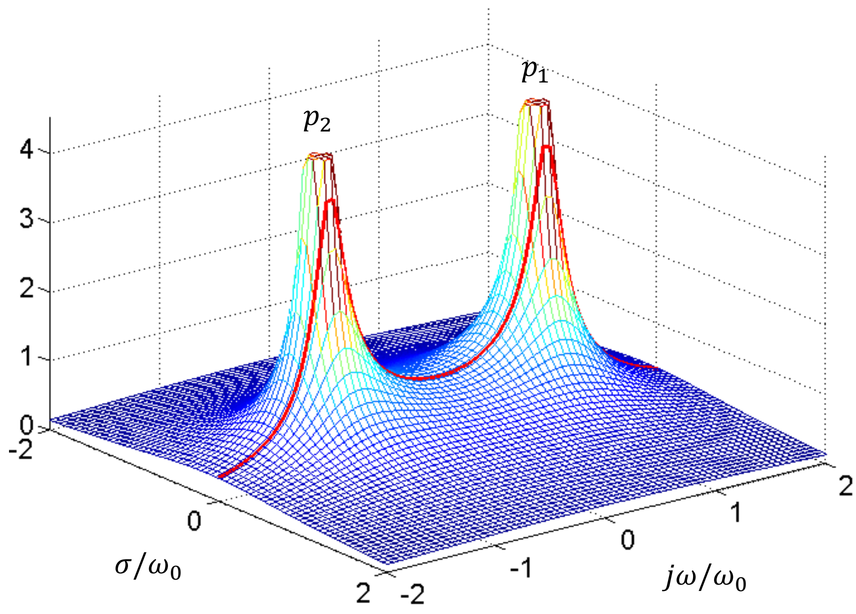
Q = 0.5


p_1, p_2
2
1.5
1
0.5
0
-2
0
σ/ω_0
2
-2
-1
0
1
2
$j\omega/\omega_0$

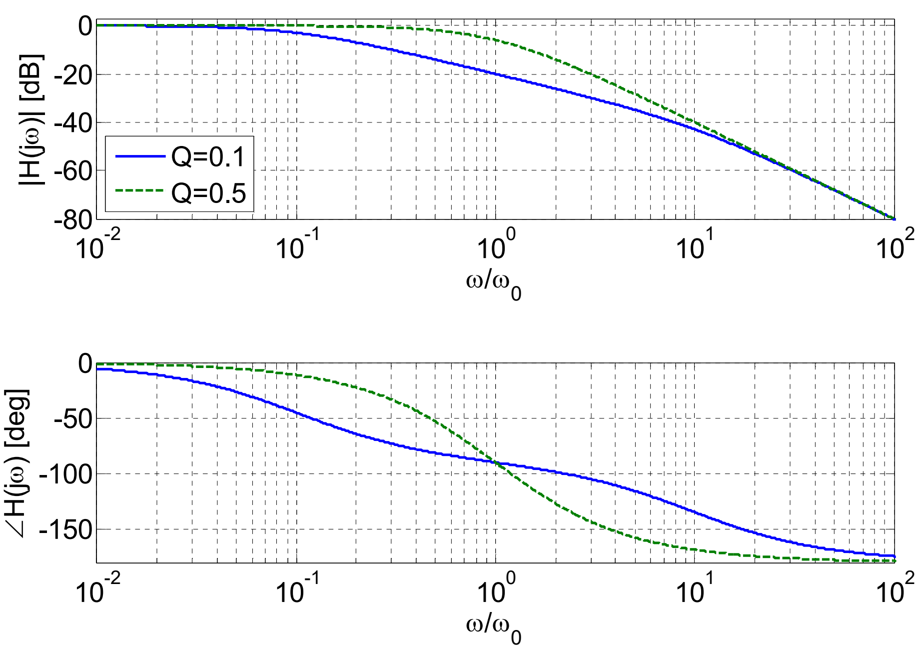
Q = 1


p_1
p_2
2
1.5
1
0.5
0
-2
0
σ/ω_0
2
-2
-1
0
1
2
$j\omega/\omega_0$

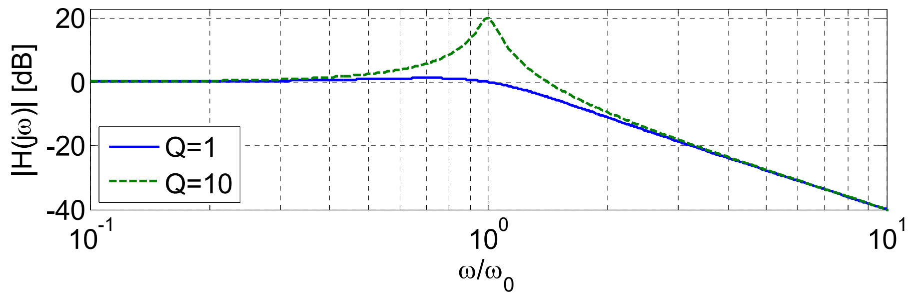
Q = 4

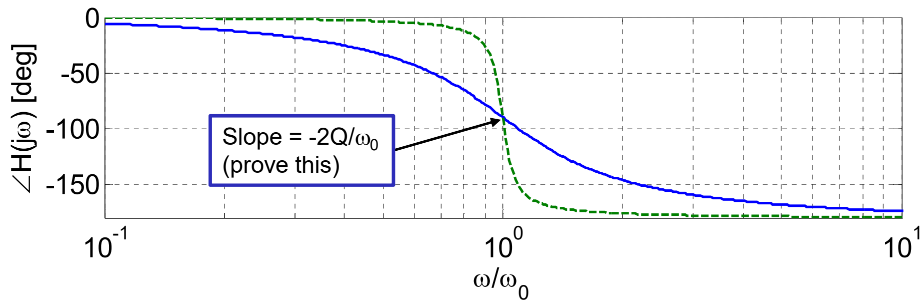


Bode Plot for Real Poles

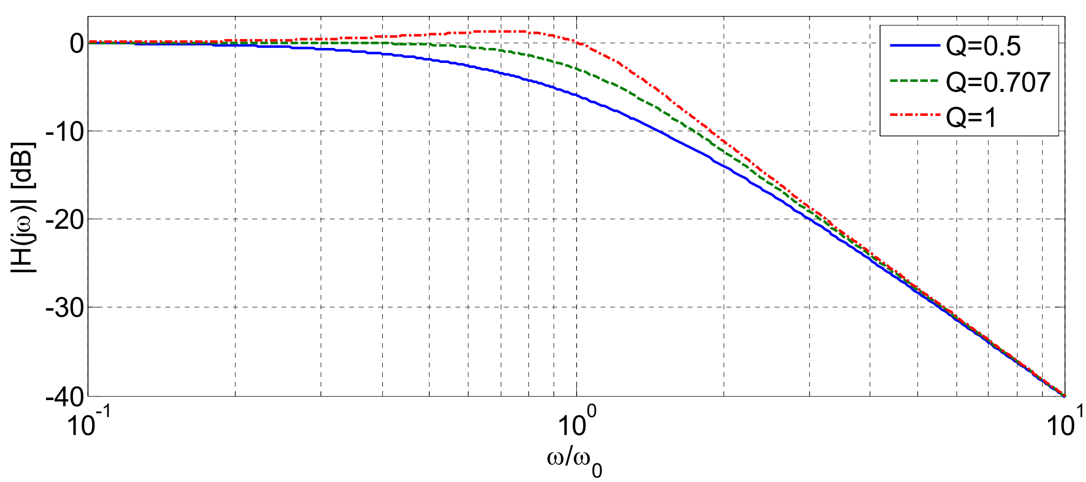


Bode Plot for Complex Poles



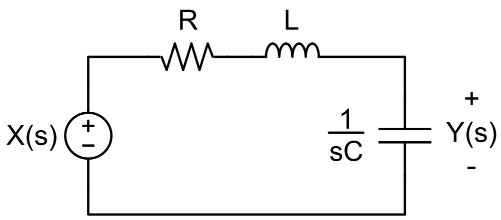


A Closer Look at the Magnitude



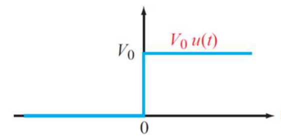
- $Q = 1/\sqrt{2}$ corresponds to a second order Butterworth response, also called "maximally flat" second order response
  - More about this when we cover filter design

Computing the Step Response



$$x(t) = V_0 u(t)$$

$$\mathcal{L}\{u(t)\} = \frac{1}{s}$$



$$Y(s) = H(s)X(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \cdot \frac{V_0}{s} = \frac{p_1 p_2}{(s-p_1)(s-p_2)} \cdot \frac{V_0}{s}$$

- First consider distinct real poles and perform a partial fraction expansion

$$Y(s) = \frac{A}{s} + \frac{B}{s-p_1} + \frac{C}{s-p_2}$$

Partial Fraction Expansion for Distinct Real Poles (Q < 0.5)

$$\frac{Y(s)}{V_0} = \frac{p_1 p_2}{(s-p_1)(s-p_2)s} = \frac{A}{s} + \frac{B}{s-p_1} + \frac{C}{s-p_2}$$

$$= \frac{A(s-p_1)(s-p_2) + B(s-p_2)s + C(s-p_1)s}{(s-p_1)(s-p_2)s}$$

$s = 0$: $\quad p_1 p_2 = A(s-p_1)(s-p_2) \qquad A = \left.\frac{p_1 p_2}{(s-p_1)(s-p_2)}\right|_{s=0} = H(0) = 1$

$s = p_1$: $\quad p_1 p_2 = B(p_1 - p_2)p_1 \qquad B = \frac{p_2}{p_1 - p_2} \qquad C = \frac{p_1}{p_2 - p_1}$

$$\frac{Y(s)}{V_0} = \frac{1}{s} + \frac{B}{s-p_1} + \frac{C}{s-p_2} \qquad \frac{y(t)}{V_0} = 1 + \underbrace{Be^{p_1 t} + Ce^{p_2 t}}_{\substack{\text{Transient response} \\ \text{(decaying exponentials)}}}$$

- Consider the special case where $|p_2| >> |p_1|$, i.e. p_1 is a dominant pole

$$B = \frac{p_2}{p_1 - p_2} \cong -1 \qquad\qquad C = \frac{p_1}{p_2 - p_1} \cong 0$$

$$\frac{y(t)}{V_0} = 1 + Be^{p_1 t} + Ce^{p_2 t} \cong 1 - e^{p_1 t}$$

- The step response approaches the same result we saw for a single pole system, with a time constant $\tau = -1/p_1$

Partial Fraction Expansion for Coincident Real Poles (Q = 0.5)

$$\frac{Y(s)}{V_0} = \frac{p^2}{(s-p)^2 s} = \frac{A}{s} + \frac{B_1}{s-p} + \frac{B_2}{(s-p)^2} = \frac{A(s-p)^2 + B_1(s-p)s + B_2 s}{(s-p)^2 s}$$

$$s = p: \qquad p^2 = B_2 p \qquad B_2 = p = -\omega_0$$

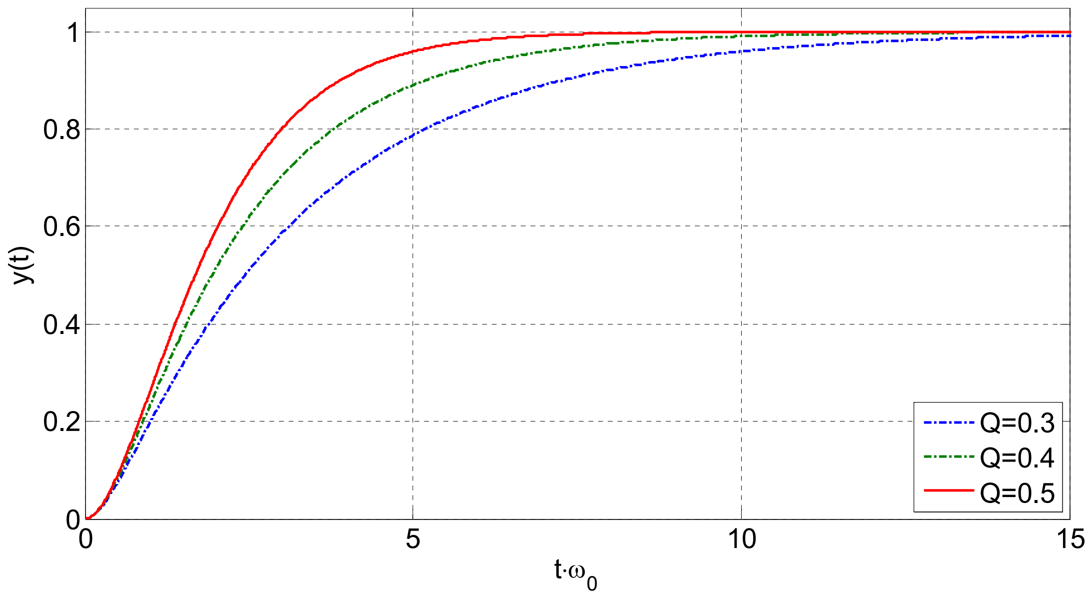
$$s = 1: \qquad p^2 = (1-p)^2 + B_1(1-p) + p \qquad B_1 = -1$$

$$\frac{Y(s)}{V_0} = \frac{1}{s} - \frac{1}{s+\omega_0} - \frac{\omega_0}{(s+\omega_0)^2} \qquad\qquad \mathcal{L}^{-1}\left\{\frac{1}{(s+a)^2}\right\} = te^{-at}$$

$$\frac{y(t)}{V_0} = 1 - (1 + \omega_0 t)e^{-\omega_0 t}$$

"Critically damped response"

Step Response for Real Poles



- The critically damped case (Q = 0.5) corresponds to the fastest possible settling without overshoot; the case for Q < 0.5 is called overdamped

Partial Fraction Expansion for Complex Conjugate Poles (Q > 0.5)

- Essentially the same algebra as for district real poles, except that we are dealing with complex conjugate roots

$$\frac{Y(s)}{V_0} = \frac{1}{s} + \frac{B}{s-p} + \frac{B^*}{s-p^*} \qquad B = \frac{p^*}{p-p^*} = \frac{p^*}{2\cdot \mathcal{Im}(p)} = |B|e^{j\theta}$$

$$\frac{y(t)}{V_0} = 1 + Be^{pt} + B^*e^{p^*t}$$

$$\mathcal{L}^{-1}\left\{\frac{e^{j\theta}}{s-(a+j\omega_d)} + \frac{e^{-j\theta}}{s-(a-j\omega_d)}\right\} = 2e^{at}\cos(\omega_d t + \theta)\,u(t)$$

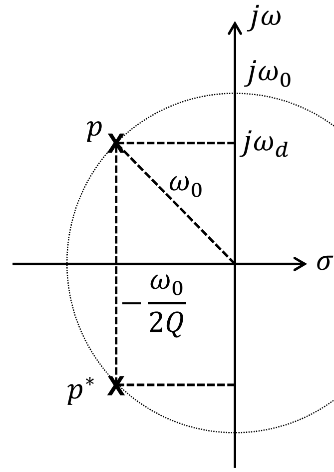
$$\frac{y(t)}{V_0} = 1 + 2|B|e^{at}\cos(\omega_d t + \phi)$$

$$a = \mathcal{Re}(p) \qquad \omega_d = \mathcal{Im}(p) \qquad \phi = \angle B$$

$$p = -\frac{\omega_0}{2Q}\left(1 - j\sqrt{4Q^2 - 1}\right) \qquad |p| = -\frac{\omega_0}{2Q}\sqrt{1^2 + 4Q^2 - 1} = \omega_0$$

$$a = \mathcal{Re}(p) = -\frac{\omega_0}{2Q}$$

Envelope decay time constant
Approaches zero for high Q

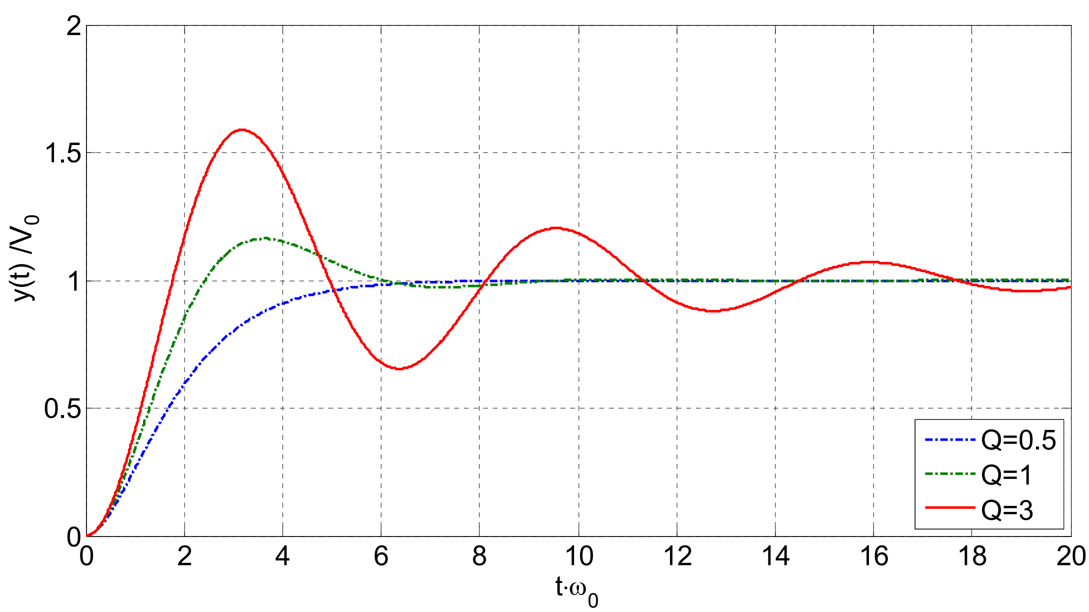


$$\omega_d = \mathcal{Im}(p) = \omega_0\sqrt{1 - \frac{1}{4Q^2}}$$

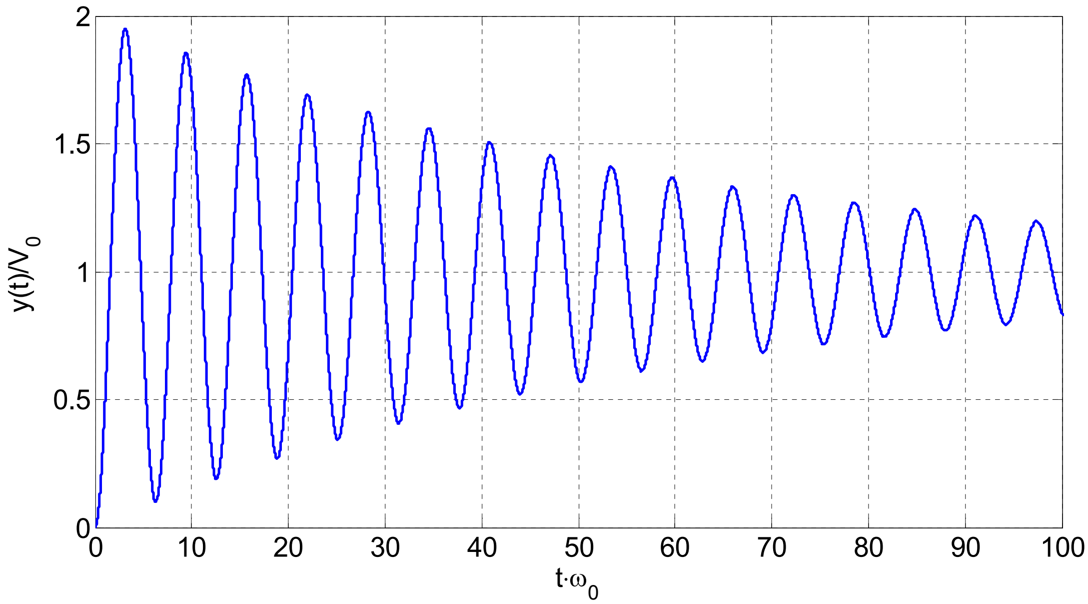
Damped frequency
Approaches ω_0 for high Q

Final Result — Step Response with Complex Poles

$$\frac{y(t)}{V_0} = 1 - \frac{\omega_0}{\omega_d} e^{-\frac{\omega_0 t}{2Q}} \sin\left[\omega_d t + acos\left(\frac{1}{2Q}\right)\right]$$

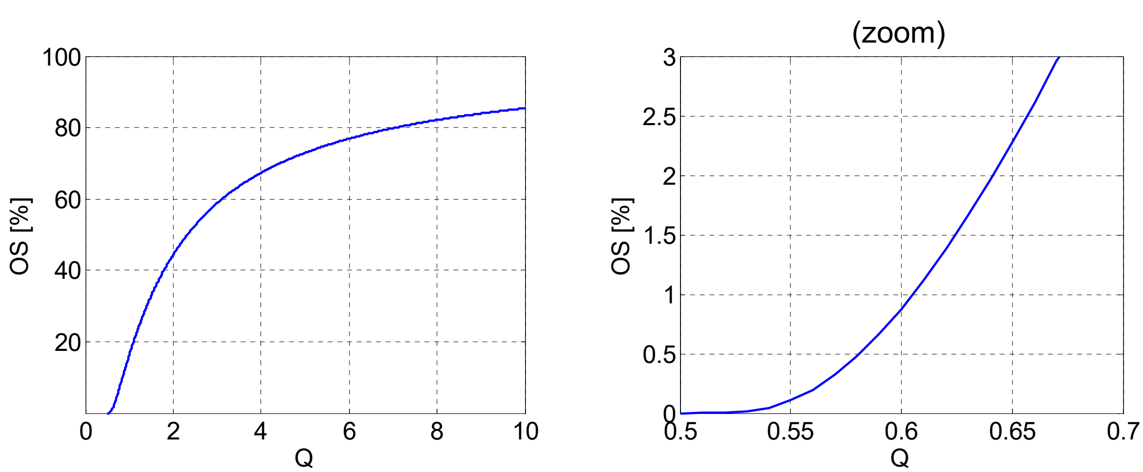


Q = 30

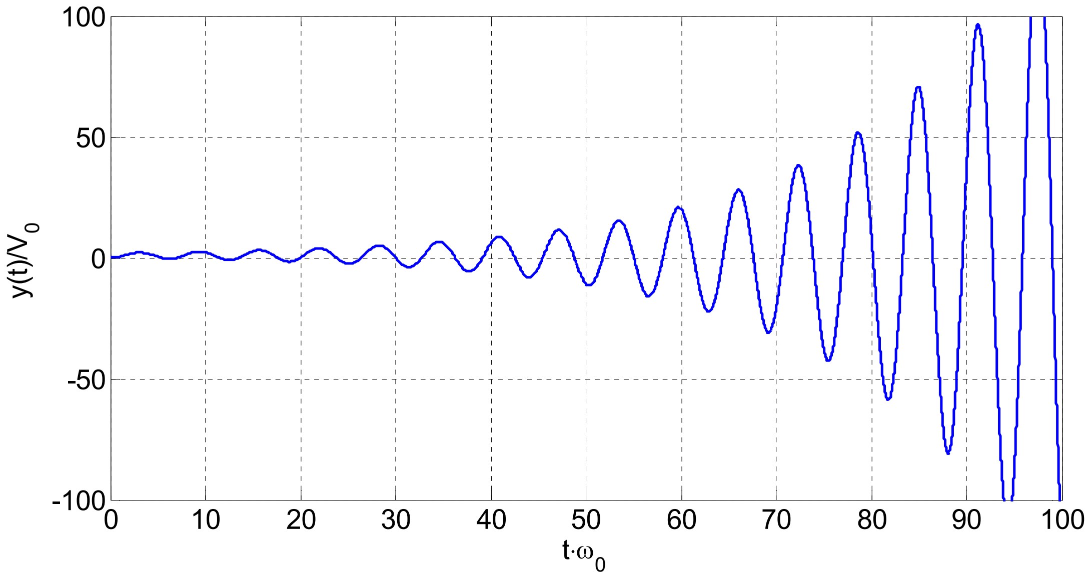


Percent Overshoot as a Function of Q

$$OS = 100\% \cdot e^{-\frac{\pi}{\sqrt{4Q^2-1}}}$$



Same Circuit with Negative Resistor



- The real part of the poles becomes positive (poles in the RHP); the sinusoid grows exponentially
- We'll get back to this when we talk about oscillators…

Chapter 10

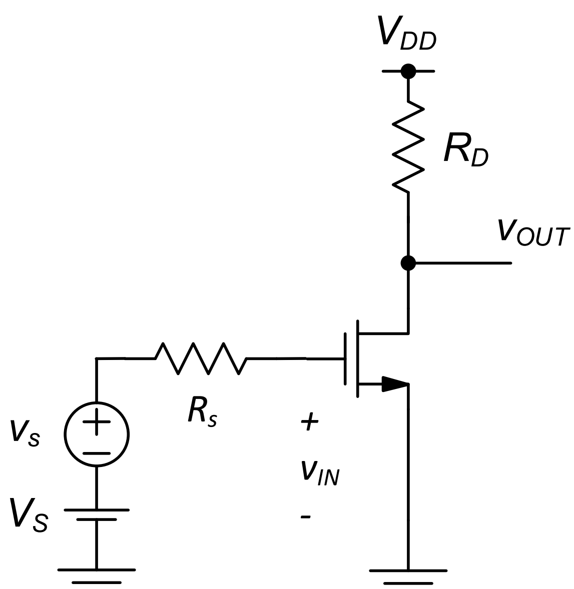
CS Stage Frequency Response

Boris Murmann

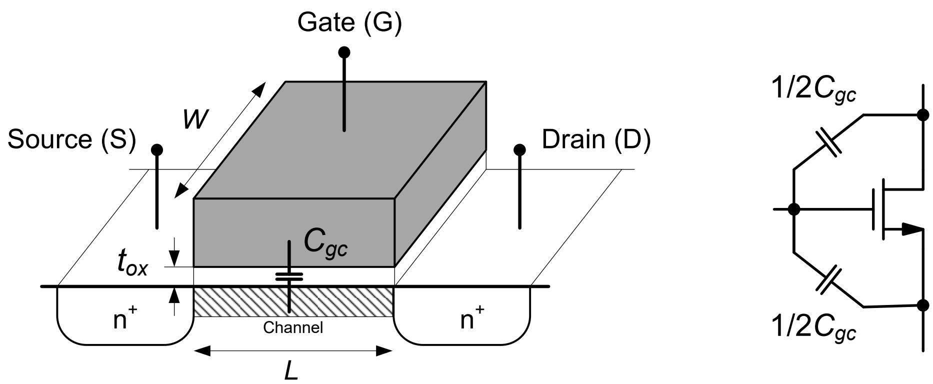
Stanford University

Reading: Murmann, Sections 3-2-1, 3-2-2, 3-3-1, 3-3-3, 3-3-4

What is the Bandwidth of this Circuit?



Intrinsic Gate Capacitance of a MOSFET (Triode Region)



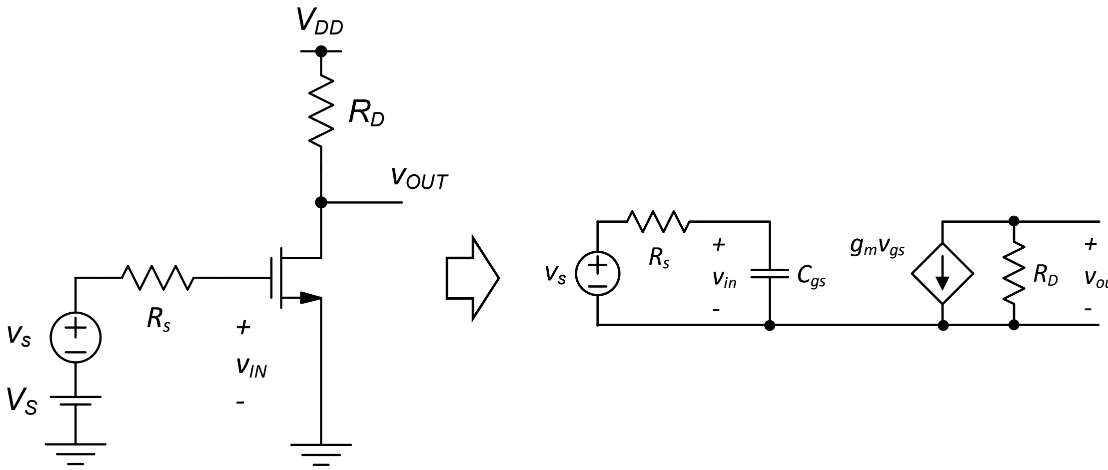
$$C_{gc} = WLC_{ox}$$

Transition to Saturation

	C_{gs}	C_{gd}
Triode	1/2 WLC_{ox}	1/2 WLC_{ox}
Saturation	2/3 WLC_{ox}	0

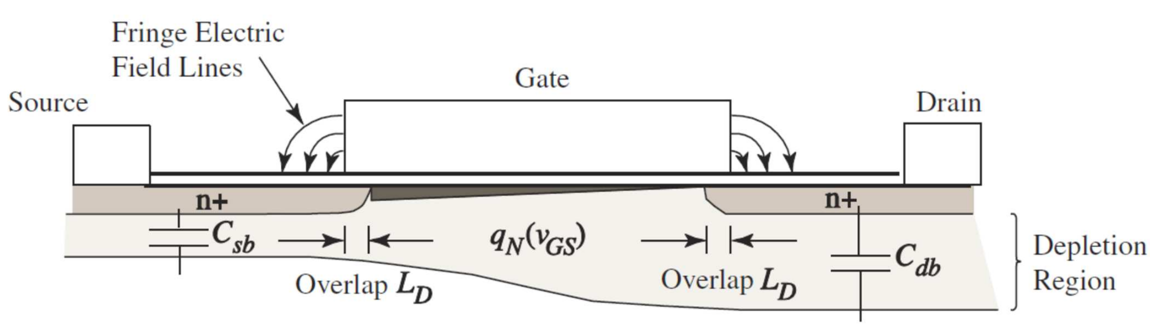
- The gate-drain capacitance goes to zero due to pinch-off
  - The channel charge becomes independent of the drain voltage
- The gate-source capacitance is less than WLC_{ox} since one end of the inversion charge "triangle" is pinned
  - The factor 2/3 comes from the geometry of the triangle

Circuit Model with Intrinsic Capacitance



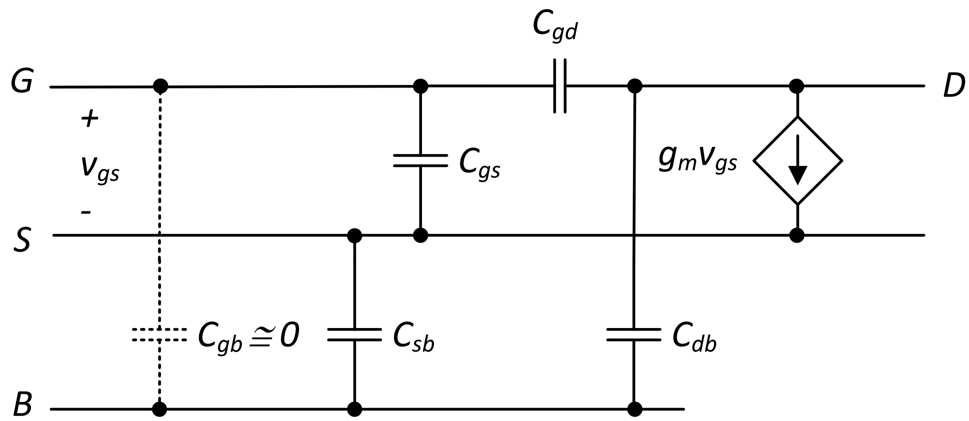
$$H(s) = \frac{v_{out}(s)}{v_s(s)} = -g_m R_D \cdot \frac{1}{1 + sR_s C_{gs}}$$

Extrinsic Capacitances

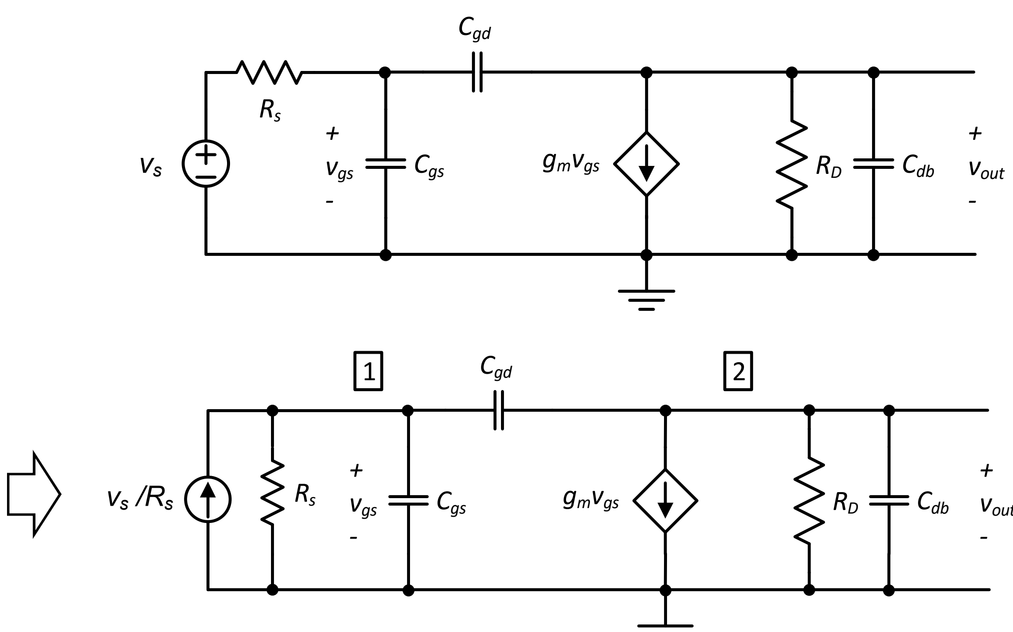


- Capacitances due to gate overlap and fringe capacitance, as well as (reverse biased) drain and source junctions
- These capacitances are classified as “extrinsic” since they are not fundamentally required for the MOSFET to function

MOSFET Model with Extrinsic Capacitances



Analysis with Extrinsic Capacitances



- Writing KCL at the circuit's two nodes and solving for v_{out}/v_s gives

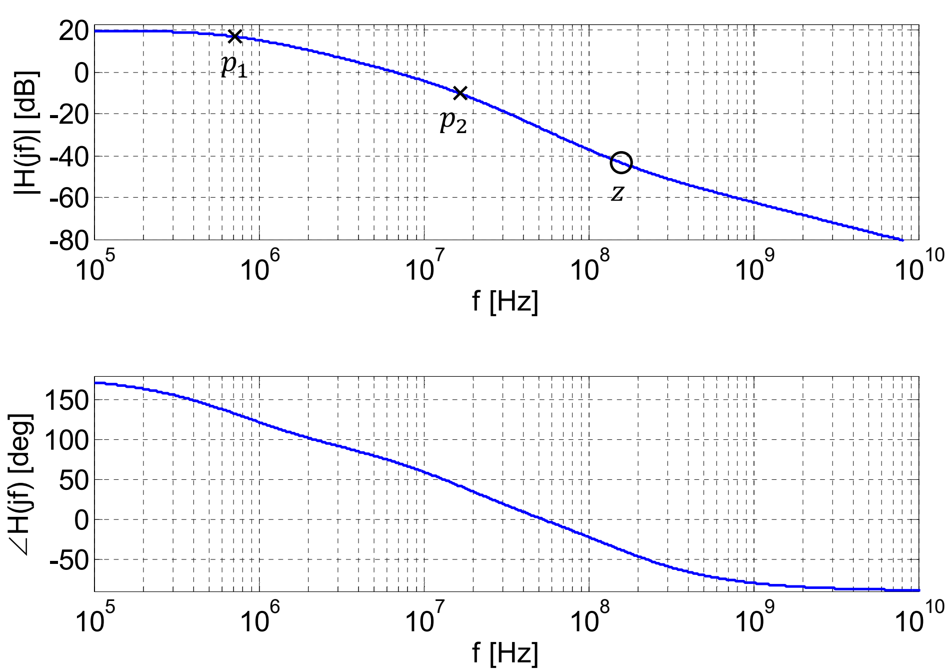
$$H(s) = \frac{v_{out}(s)}{v_s(s)} = -g_m R_D \cdot \frac{1 - s\dfrac{C_{gd}}{g_m}}{1 + b_1 s + b_2 s^2}$$

$$b_1 = C_{gs}R_s + C_{gd}(R_s + R_D + g_m R_D R_s) + C_{db}R_D$$

$$b_2 = R_s R_D(C_{gs}C_{gd} + C_{gs}C_{db} + C_{gd}C_{db})$$

- Pretty messy!
- Only thing we can see clearly at this point is that the circuit has a RHP zero at high frequencies
  - What causes this zero?
- Let's plug in some typical numbers to see what this response looks like

$g_m = 1mS, R_s = R_D = 10k\Omega, C_{gs} = 10pF, C_{gd} = C_{db} = 1pF$ $\qquad f_z = \frac{1}{2\pi}\frac{g_m}{C_{gd}} = 159MHz$

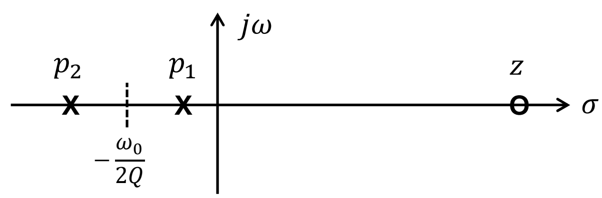


Observations

- The circuit has two real poles that are quite far apart
  - A low-Q system

$$H(s) = G \cdot \frac{1 - \frac{s}{z}}{1 + b_1 s + b_2 s^2} = G \cdot \frac{1 - \frac{s}{z}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \frac{1}{\sqrt{b_2}} = 21.82 \frac{Mrad}{sec} \qquad Q = \frac{\sqrt{b_2}}{b_1} = 0.199$$



The Dominant Pole Approximation

- If all we want to know about the circuit is it's 3-dB bandwidth, it is clear that both p_2 and z are irrelevant
- Given $|p_2| >> |p_1|$, we can approximate the denominator as follows

$$\frac{1}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} = \frac{1}{1 - \frac{s}{p_1} - \cancel{\frac{s}{p_2}} + \frac{s^2}{p_1 p_2}} \cong \frac{1}{1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}}$$

$$\frac{1}{1 + b_1 s + b_2 s^2} \cong \frac{1}{1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}}$$

$$\boxed{p_1 \cong -\frac{1}{b_1}} \qquad p_2 \cong -\frac{b_1}{b_2}$$

Resulting Bandwidth Estimate

- All we need to estimate the bandwidth of this circuit is b_1!

$$|H(s)|_{s=j2\pi f_{3dB,actual}} = \frac{1}{\sqrt{2}} \qquad \Rightarrow f_{3dB,actual} = 736kHz$$

$$f_{3dB,estimate} \cong \frac{1}{2\pi}\frac{1}{b_1} = 692kHz \qquad Error = \frac{736-692}{736} = -5.9\%$$

- Pretty good, especially given that it is very painful to solve for the exact corner frequency
- Important question at this point: Is there an “easy” way to compute b_1 without grinding through KCL?
  - Yes! We can apply the method of open-circuit time constants (OCTC)

Chapter 11

Open-Circuit Time Constant Analysis

Boris Murmann

Stanford University

Reading: Murmann, Section 3-4

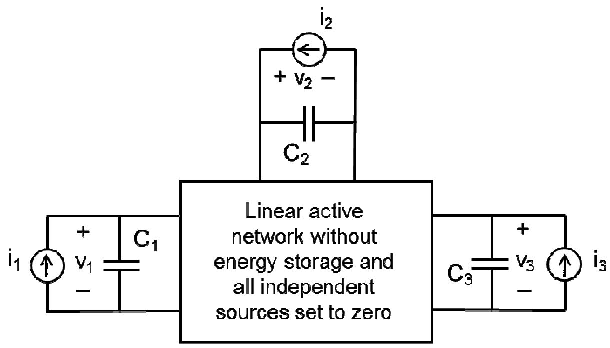
Open-Circuit Time Constant (OCTC) Analysis

- Also called "Zero-Value Time Constant (ZVTC) Analysis"
- Developed in the mid 1960s at MIT
- A step-by-step circuit analysis method that allows us to determine b_1 (and only b_1) without solving for the complete transfer function
- Here's how it works
  - Remove all but one capacitor (C_j)
  - Short independent voltage sources
  - Remove independent current sources
  - Calculate resistance seen by capacitor (R_{jo}) and compute $\tau_{jo} = R_{jo}C_j$
  - Repeat above steps for all remaining capacitors in the circuit
  - The sum of all τ_{jo} equals b_1

$$H(s) = \frac{N(s)}{1 + b_1 s + b_2 s^2 + b_3 s^3 + \cdots} \qquad b_1 = \sum \tau_{jo} \qquad \omega_{-3dB} \cong \frac{1}{b_1}$$

Verification for an Arbitrary Three-Port Network

- Consider a linear active circuit containing only capacitors as energy storage elements
- The math can be easily extended to N ports



$$i_1 = (g_{11} + sC_1)v_1 + g_{12}v_2 + g_{13}v_3$$
$$i_2 = g_{21}v_1 + (g_{22} + sC_2)v_2 + g_{23}v_3$$
$$i_3 = g_{31}v_1 + g_{32}v_2 + (g_{33} + sC_3)v_3$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \underbrace{\begin{bmatrix} g_{11} + sC_1 & g_{12} & g_{13} \\ g_{21} & g_{22} + sC_2 & g_{23} \\ g_{31} & g_{32} & g_{33} + sC_3 \end{bmatrix}}_{G} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

- As an example, say we declared port 1 as our input (and i_1 as an independent source) and v_3 as our output
- How can we find the transfer function v_3/i_1?
- One way is to use Cramer's rule

$$v_3 = \frac{\det(G_3)}{\det(G)} = \frac{\Delta_3}{\Delta} \qquad G_3 = \begin{bmatrix} g_{11} & g_{12} & i_1 \\ g_{21} & g_{22} + sC_2 & 0 \\ g_{31} & g_{32} & 0 \end{bmatrix}$$

$$\frac{v_3}{i_1} = \frac{Some\ Numerator}{\det(G)}$$

- Key take-home: The denominator of the transfer function is given by the determinant of the network matrix
  - This means that we should be able to find b_1 from the determinant of G

$$\Delta = \begin{vmatrix} g_{11}+sC_1 & g_{12} & g_{13} \\ g_{21} & g_{22}+sC_2 & g_{23} \\ g_{31} & g_{32} & g_{33}+sC_3 \end{vmatrix} = k_0 + k_1 s + k_2 s^2 + k_3 s^3 = k_0(1 + b_1 s + \cdots)$$

$$b_1 = \frac{k_1}{k_0} \qquad k_0 = \Delta\Big|_{C_1=C_2=C_3=0}$$

How to find k_1? Expand determinant by each row to find contributions from each C_i

$$k_1 = h_1 sC_1 + h_2 sC_2 + h_3 sC_3$$

$$\Delta = (g_{11}+sC_1)\begin{vmatrix} g_{22}+sC_2 & g_{23} \\ g_{32} & g_{33}+sC_3 \end{vmatrix} - g_{12}\begin{vmatrix} g_{21} & g_{23} \\ g_{31} & g_{33}+sC_3 \end{vmatrix} + g_{13}\begin{vmatrix} g_{21} & g_{22}+sC_2 \\ g_{31} & g_{32} \end{vmatrix}$$

$$\Rightarrow h_1 = \Delta_{11}\Big|_{C_2=C_3=0}$$

$$\boxed{k_1 = C_1\Delta_{11}|_{C_2=C_3=0} + C_2\Delta_{22}|_{C_1=C_3=0} + C_3\Delta_{33}|_{C_1=C_2=0}}$$

$$b_1 = \frac{k_1}{k_0} = C_1\frac{\Delta_{11}}{\Delta}\Big|_{C_i=0} + C_2\frac{\Delta_{22}}{\Delta}\Big|_{C_i=0} + C_3\frac{\Delta_{33}}{\Delta}\Big|_{C_i=0}$$

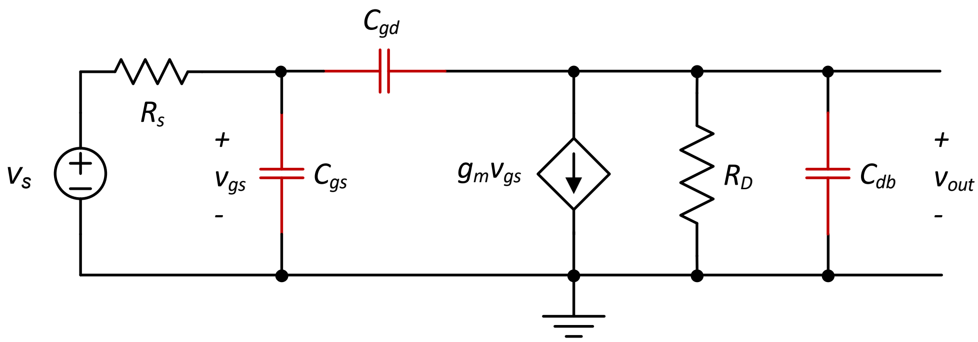
- Finally, note that the terms that multiply the capacitances are really just the resistances looking into the respective ports with all capacitors removed
- To see this, apply a test current i_1, let $i_2 = i_3 = 0$, $C_1 = C_2 = C_3 = 0$ and compute $R_{1o} = v_1/i_1$

$$v_1 = \frac{\Delta_1}{\Delta} = i_1\frac{\Delta_{11}}{\Delta} \qquad \Delta_1 = \begin{bmatrix} i_1 & g_{12} & g_{13} \\ 0 & g_{22}+sC_2 & g_{23} \\ 0 & g_{32} & g_{33}+sC_3 \end{bmatrix} = i_1\Delta_{11}$$

$$Z_1 = \frac{v_1}{i_1} = \frac{\Delta_{11}}{\Delta} \qquad R_{1o} = \frac{v_1}{i_1} = \frac{\Delta_{11}}{\Delta}\Big|_{C_i=0}$$

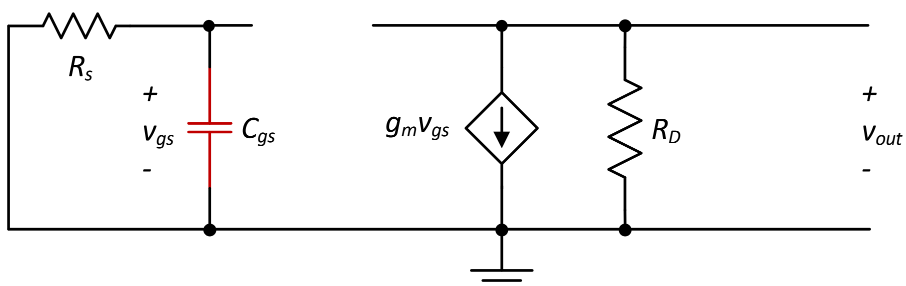
$$\boxed{b_1 = C_1R_{1o} + C_2R_{2o} + C_3R_{3o}}$$

Application to Our CS Stage Example



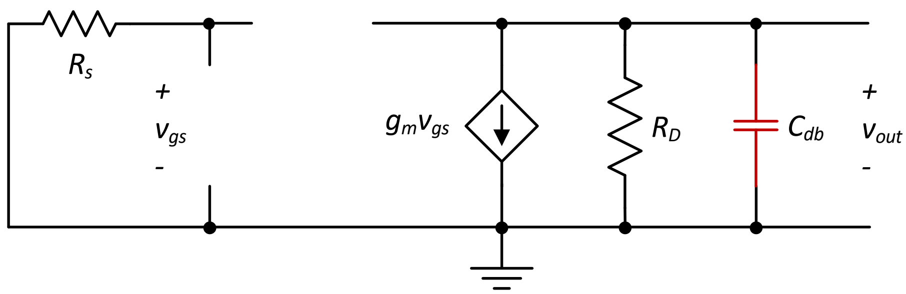
- Three capacitors, so we need to run three OCTC calculations

Calculation for C_{gs}



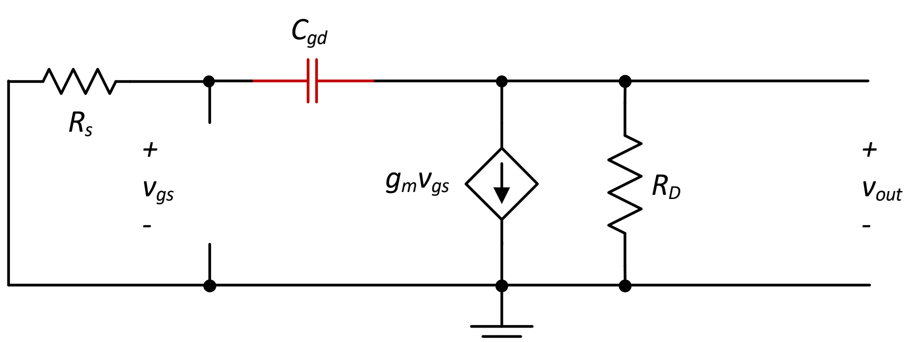
$$\tau_{gso} = R_s C_{gs}$$

Calculation for C_{db}

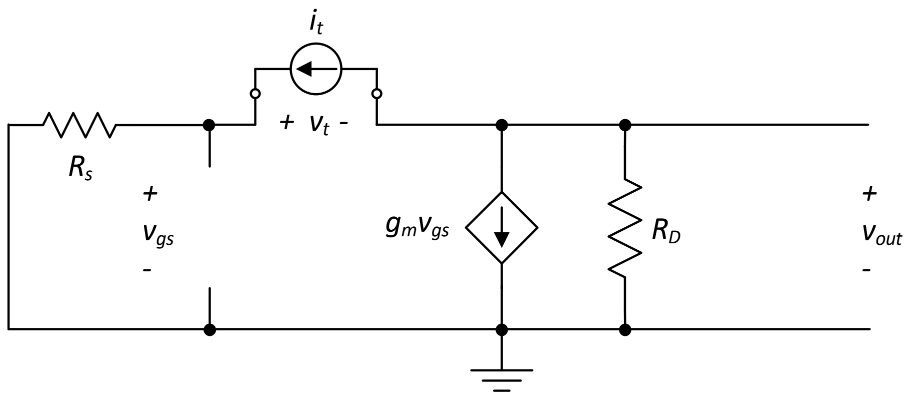


$$\tau_{dbo} = R_D C_{db}$$

Calculation for C_{gd}



- Result is not obvious at first glance
- Must go back to first principles
  - Inject a test current, measure voltage



$$v_t = v_{gs} + R_D\left(g_m v_{gs} + i_t\right) = i_t R_S + R_D(g_m i_t R_S + i_t)$$

$$R_{gdo} = \frac{v_t}{i_t} = R_S + R_D + g_m R_S R_D \qquad \tau_{gdo} = (R_S + R_D + g_m R_S R_D)C_{gd}$$

"$R_{left} + R_{right} + g_m R_{left} R_{right}$"

Putting it All Together

$$b_1 = \sum \tau_{jo} = R_s C_{gs} + (R_s + R_D + g_m R_D R_s)C_{gd} + R_D C_{db}$$

$$\omega_{-3dB} \cong \frac{1}{b_1}$$

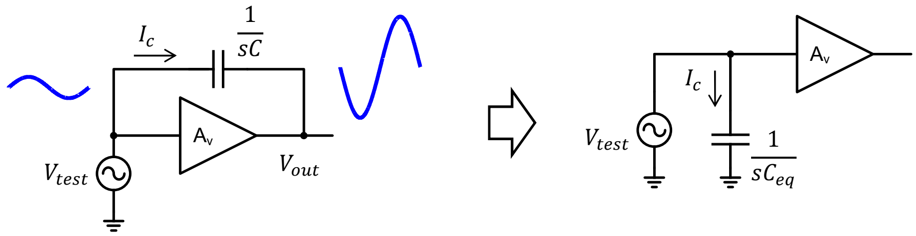
- Same result we got from the full KCL-based analysis of the CS stage
  - But without the pain of doing the full-blown analysis
- Another nice feature of this analysis is that we can inspect the circuit nicely for potential bottlenecks
  - Using the previous numbers, we see:

$$g_m = 1mS, R_s = R_D = 10k\Omega, C_{gs} = 1pF, C_{gd} = C_{db} = 0.1pF$$

$\tau_{gso} = R_s C_{gs} = 100ns$	$\tau_{dbo} = R_D C_{db} = 10ns$	$\tau_{gdo} = (R_S + R_D + g_m R_D R_S)C_{gd} = 120ns$
significant	negligible	most significant

A Closer Look at τ_{gdo}

- Even though C_{gd} is relatively small, the associated time constant is the largest in the circuit – what's going on here?
- The issue has to do with the so-called Miller effect



$$I_c = sC(V_{test} - A_v V_{test}) \qquad \frac{I_c}{V_{test}} = sC(1 - A_v) = sC_{eq} \qquad C_{eq} = C(1 - A_v)$$

- If A_v is negative, the capacitance is seen "amplified" by $1 + |A_v|$
- This effect is studied in much more detail in EE114

Important Notes on OCTC

- The key advantages of this method are
  - It provides a shortcut for finding the -3dB frequency of a circuit
  - It provides us with insight about the limiting time constants!
- Whenever you apply the OCTC method, it is important to remember the assumptions for which it is accurate
  - The circuit has a dominant pole and no zeros nearby
  - The circuit does not have any high-Q complex poles
- Interestingly, when these underlying assumptions are not precisely met, it may still be "OK" to work with OCTCs
  - See examples on the following slides
- A common pitfall has to do with AC coupling caps or bypass caps
  - Meant to be "shorts" at high frequencies, and do not degrade the signal bandwidth
  - Simply ignore such caps in your OCTC analysis

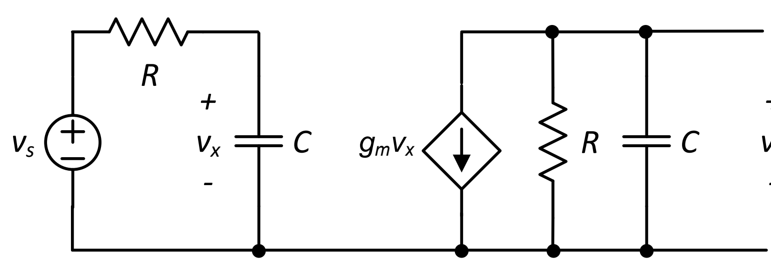
And Finally…

Open Circuit Time Constants do not

(necessarily)

correspond to poles!

Example: Circuit With Two Identical Poles



- Exact calculation of the -3dB frequency

$$\frac{v_o(s)}{v_s(s)} = -\frac{g_m R}{(1+sRC)^2} \qquad \frac{1}{\sqrt{2}} = \frac{1}{1+(\omega_{3dB}RC)^2}$$

$$\omega_{3dB} = \frac{\sqrt{\sqrt{2}-1}}{RC} = \frac{0.64}{RC}$$

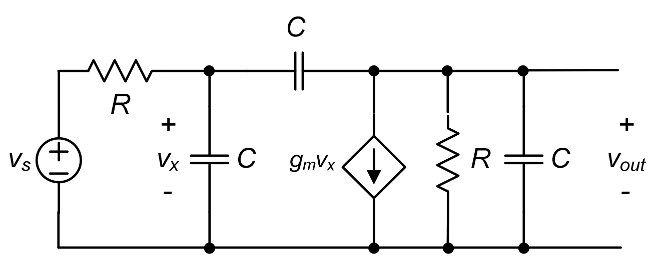
- On the other hand, running an OCTC analysis gives

$$\omega_{3dB} \cong \frac{1}{\sum \tau} = \frac{1}{RC + RC} = \frac{0.5}{RC}$$

$$Error = \frac{0.5 - 0.64}{0.5} = -22\%$$

- Observations
  – The OCTC result is conservative; the actual bandwidth is somewhat larger. This tends to hold in general, and engineers like this!
- Note that in this example the OCTCs correspond to the pole frequencies (the circuit has two poles at -1/RC)
  – This is rarely the case in more interesting circuits
  – In any circuit with a capacitive loop, the OCTCs **do not** correspond to the pole frequencies

Example: Circuit with Capacitive Loop



$$g_m R = 2$$

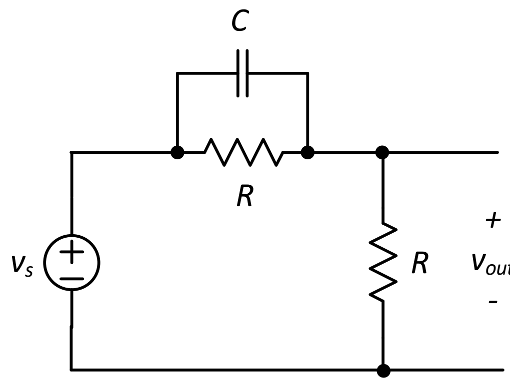
$$\sum \tau = b_1 = RC + RC + \left(R + R + g_m R^2\right)C = 6RC$$

$$b_2 = 3(RC)^2$$

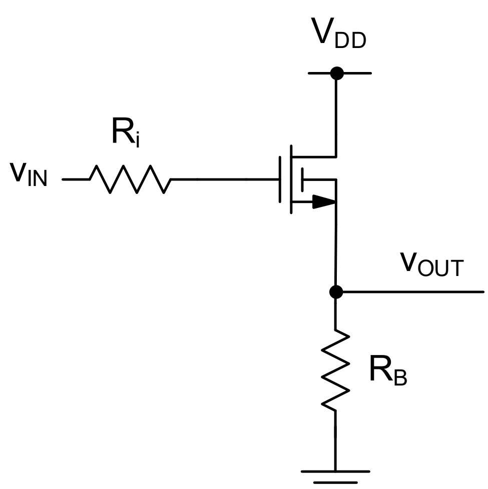
$$1 + b_1 s + b_2 s^2 = 0 \qquad \Rightarrow p_{1,2} = -\frac{1}{RC}\left(1 \pm \sqrt{\frac{2}{3}}\right) \qquad p_1 \cong -\frac{0.18}{RC}$$

- The time constants do not correspond to the poles
- The OCTC bandwidth estimate (0.167/RC) is again somewhat lower than the actual bandwidth (~0.18/RC)

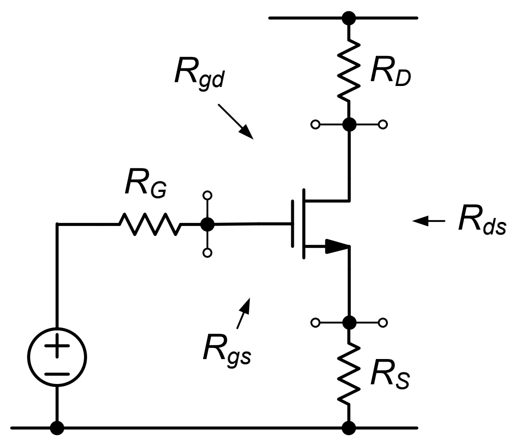
Example: Miserable Failure of OCTC



Example: Common-Drain Stage



Handy Formulas



$$R_{ds} = \frac{R_D + R_S}{1 + g_m R_S}$$

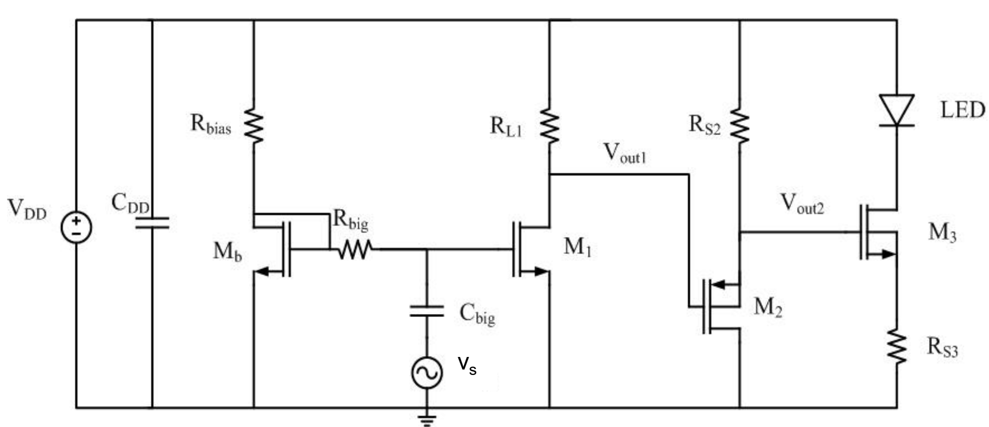
$$R_{gs} = \frac{R_G + R_S}{1 + g_m R_S}$$

$$R_{gd} = R_G + R_D + G_m R_G R_D$$

$$G_m = \frac{g_m}{1 + g_m R_S}$$

(Note: These expressions neglect finite r_o and backgate effect)

Example: Coupling Capacitor



Chapter 12

Basic Analysis of Opamp Circuits

Boris Murmann

Stanford University

References:
Ulaby & Maharbiz, Chapter 4
"Op Amps for Everyone" by Texas Instruments, Chapter 3

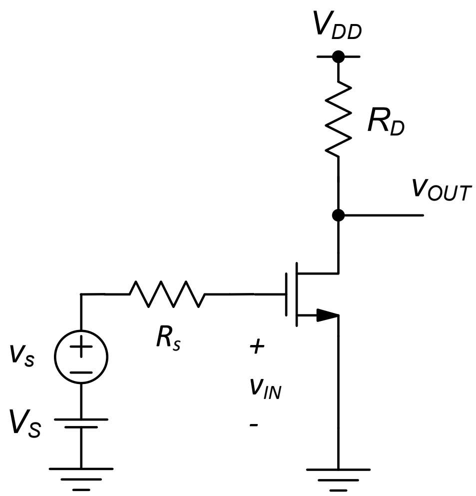
Ray Stata, Vice President
Analog Devices, Inc., Cambridge, Mass.

(Electromechanical Design, Nov. 1965)

The term "operational amplifier" was orginally coined by those in the analog computer field to denote an amplifier circuit which performed various mathematical operations such as integration, differentiation, summation and subtraction. Although operational amplifiers are still widely used for analog computation, the application of these devices has been so vastly extended that the terminology is now archaic. Today, the widest use of operational amplifiers is in such applications as signal conditioning, servo and process controls, analog instrumentation and system design, impedance transformation, voltage and current regulators and a host of other routine functions.

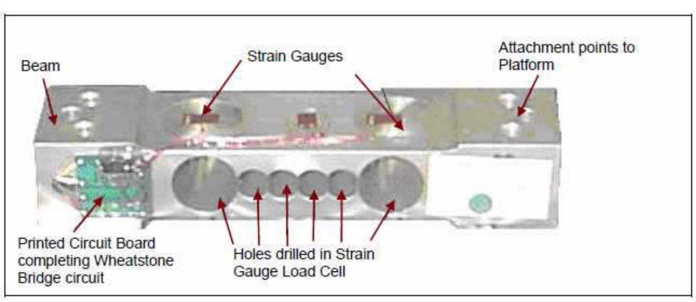
Non-linear applications of operational amplifiers have also been added to the growing frontier of analog amplifier technology. In this category, operational amplifiers are used for voltage comparators, A to D and D to A converters, logarithmic amplifiers, non-linear function generators and ultra-linear rectifiers, to name only a few applications.

Motivation



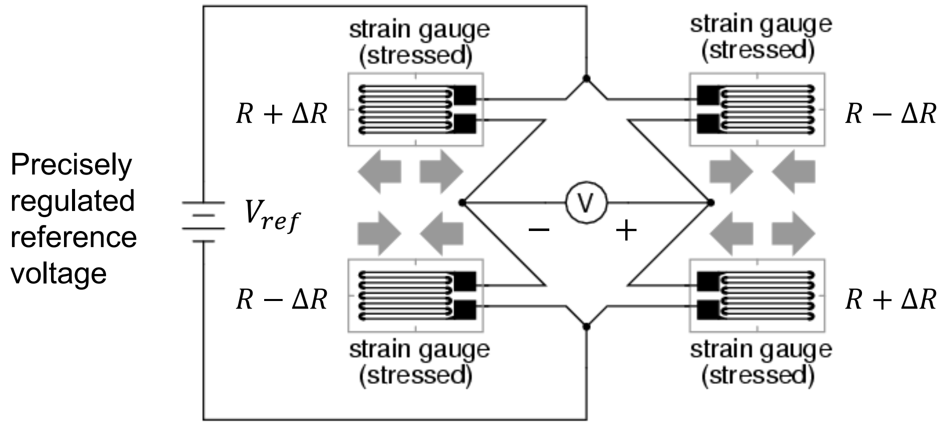
- We know how to build basic gain stages
- But, none of the circuits we have looked at so far have "precisely" controlled characteristics
- Parameters like g_m are not well defined and cause large variability
- This can be a problem for many applications
  – Let's look at an example

$$A_v = -g_m R_D$$



http://www.phantomscales.com/ohaus/valor1000.php

Full-bridge strain gauge circuit

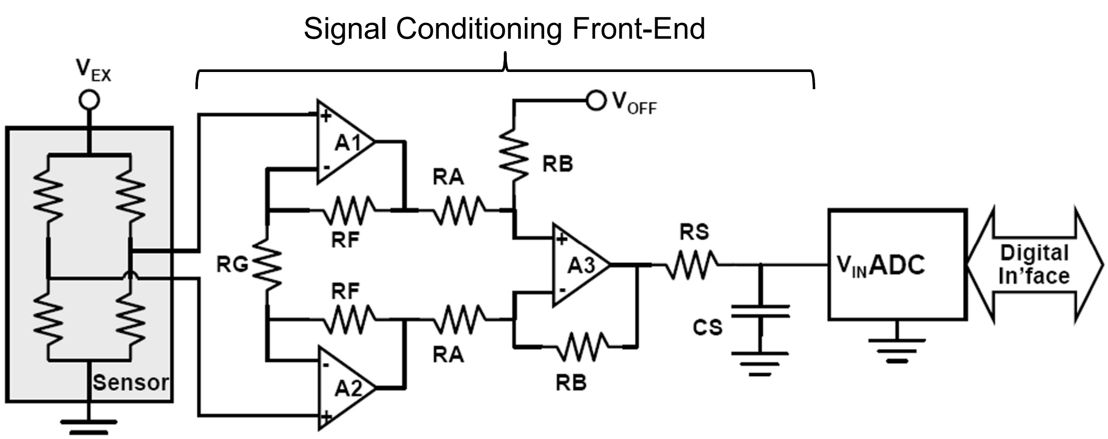


"Wheatstone Bridge"

$$V = \left(\frac{R + \Delta R}{2R} - \frac{R - \Delta R}{2R}\right) V_{ref} = \frac{\Delta R}{R} V_{ref}$$

http://www.allaboutcircuits.com/vol_1/chpt_9/7.html

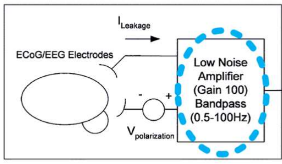
Typical Readout Circuit

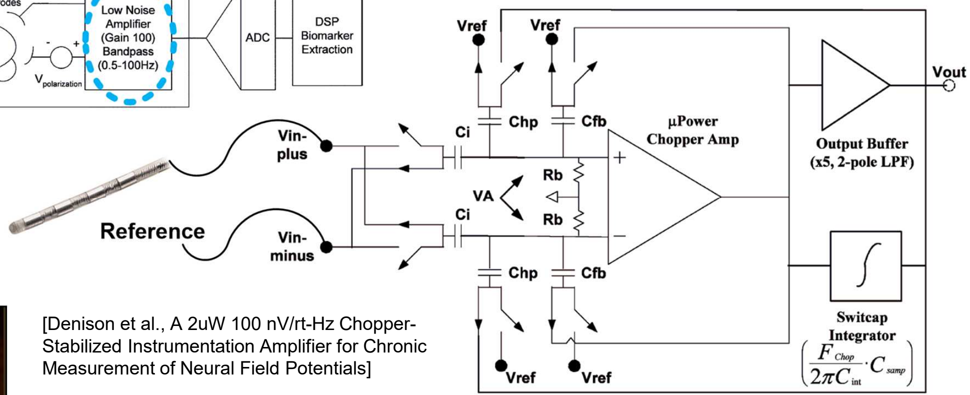


"Instrumentation Amplifier"

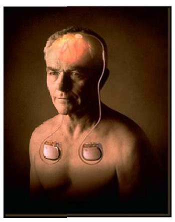
http://www.planetanalog.com/document.asp?doc_id=527950

Bio Instrumentation Amplifier IC

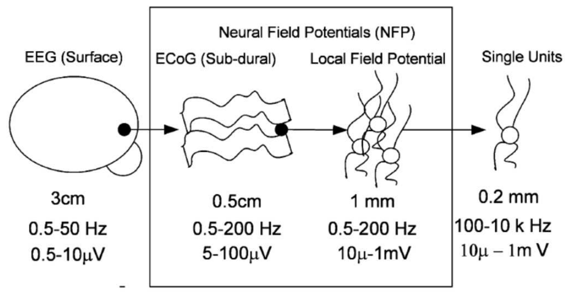


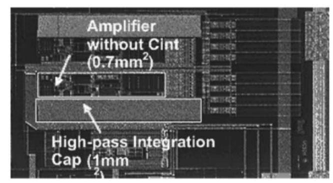


[Denison et al., A 2uW 100 nV/rt-Hz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials]

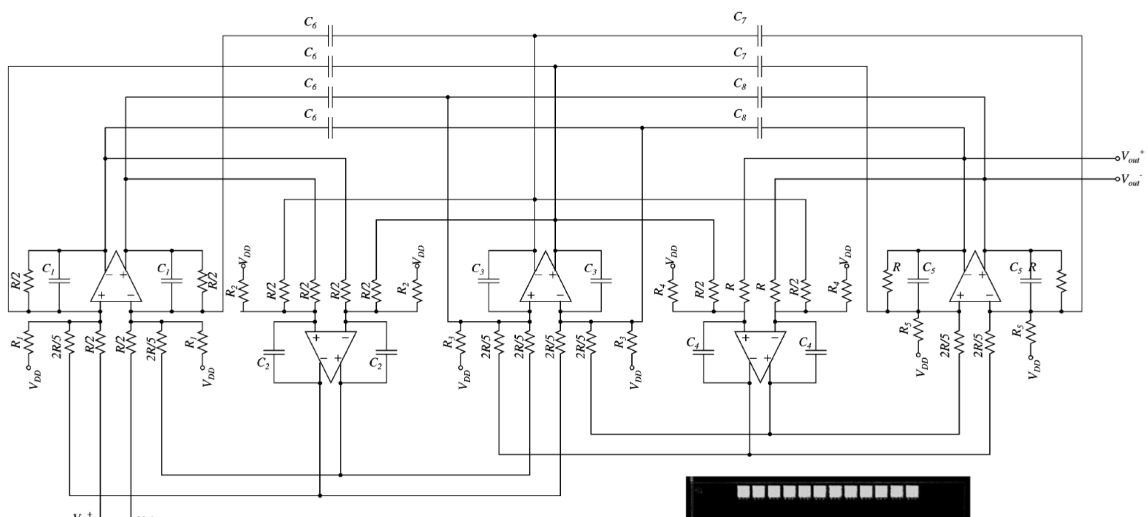


Medtronic

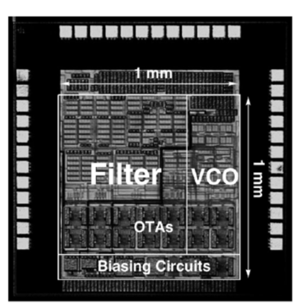




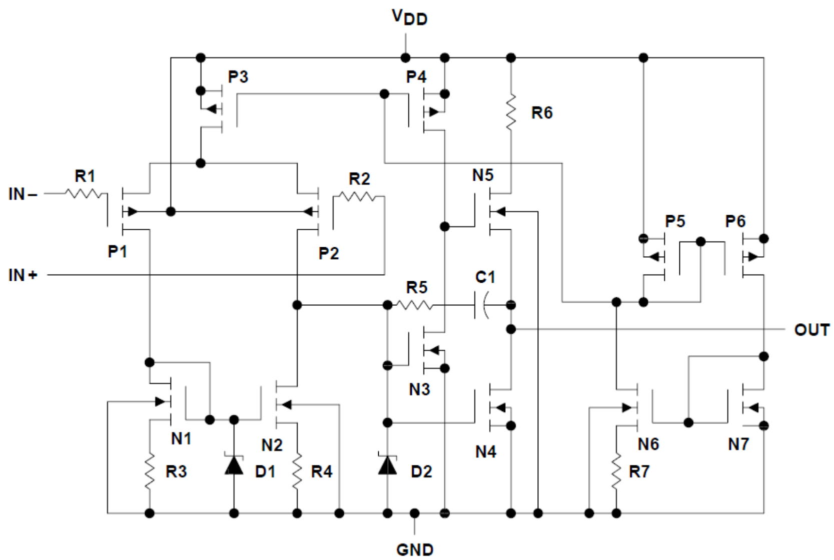
Fifth Order Lowpass Filter

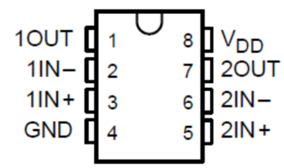


[S. Chatterjee et al., "0.5-V analog circuit techniques and their application in OTA and filter design"]

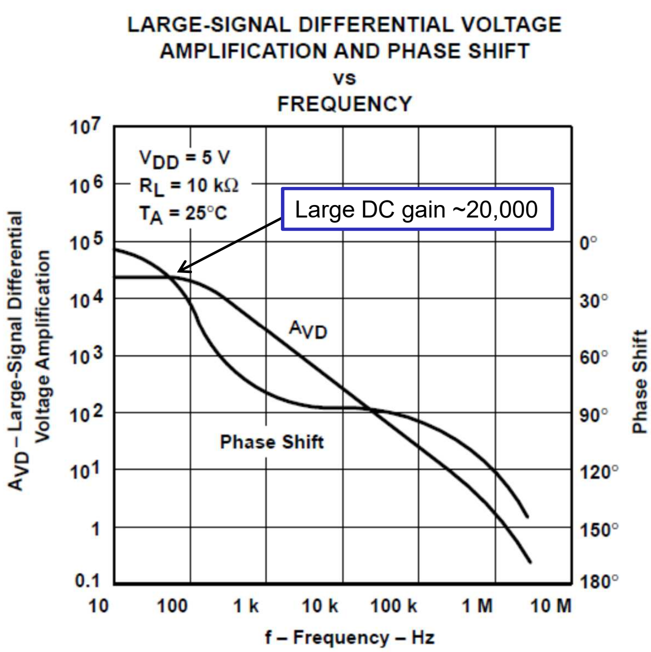


Typical (Discrete) Operational Amplifier



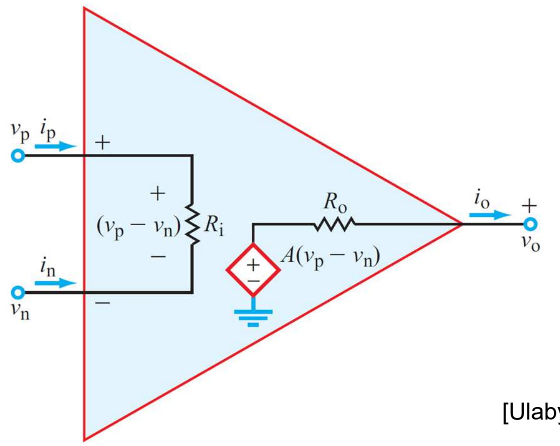


Key Characteristics



- Huge input impedance ~$10^{12}\Omega$
- Small output impedance ~300Ω

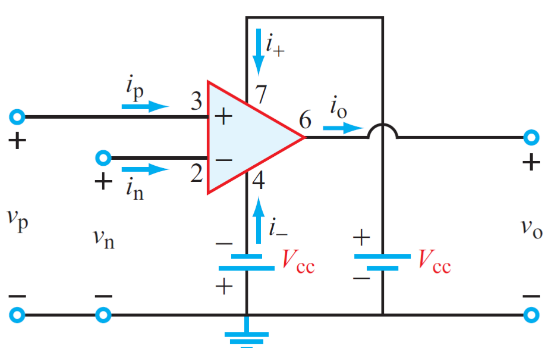
Equivalent Circuit for Low-Frequency, Small-Signal Analysis

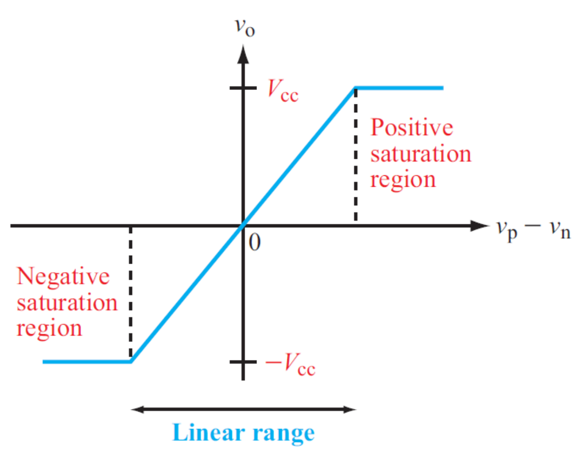


[Ulaby & Maharbiz]

Op-Amp Characteristics	Parameter	Typical Range	Ideal Op Amp
• Linear input–output response	Open-loop gain A	10^4 to 10^8 (V/V)	∞
• High input resistance	Input resistance R_i	10^6 to 10^{13} Ω	∞ Ω
• Low output resistance	Output resistance R_o	1 to 100 Ω	0 Ω
• Very high gain	Supply voltage V_{cc}	5 to 24 V	As specified by manufacturer

Large Signal Transfer Characteristic



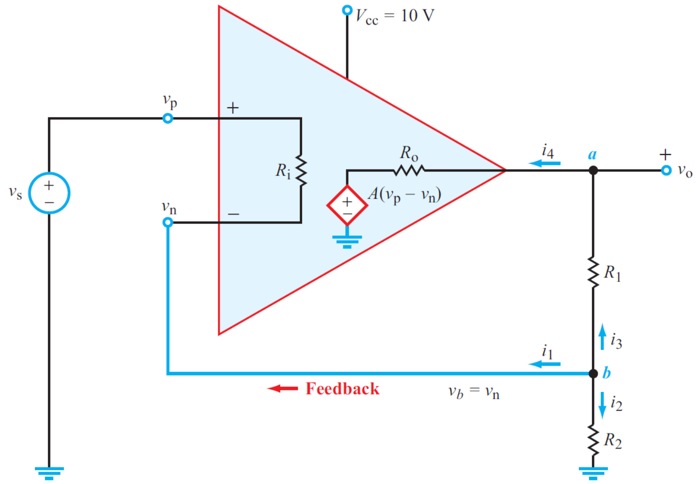


[Ulaby & Maharbiz]

First Circuit Example

For $V_{cc} = 10$ V, $A = 10^6$, $R_i = 10^7$ Ω, $R_o = 10$ Ω, $R_1 = 80$ kΩ, and $R_2 = 20$ kΩ,

[Ulaby & Maharbiz]



KCL at Node a:

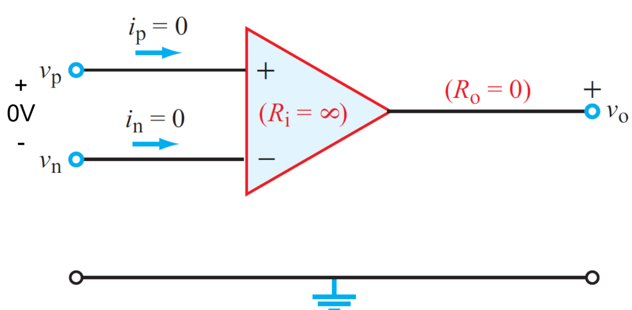
$$\frac{v_n - v_o}{R_1} = \frac{v_o - A(v_p - v_n)}{R_o}$$

KCL at Node b:

$$\frac{v_n - v_p}{R_i} + \frac{v_n}{R_2} + \frac{v_n - v_o}{R_1} = 0$$

$$G = \frac{v_o}{v_s} = \frac{[AR_i(R_1 + R_2) + R_2 R_o]}{AR_2 R_i + R_o(R_2 + R_i) + R_1 R_2 + R_i(R_1 + R_2)} = 4.999975$$

Ideal Op-Amp Approximation



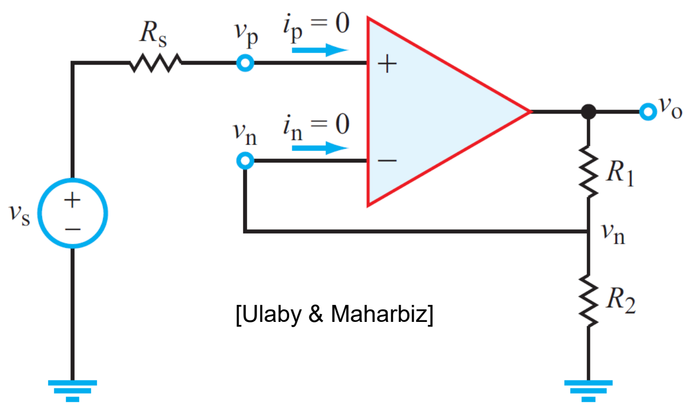
Ideal Op Amp

- Current constraint $i_p = i_n = 0$
- Voltage constraint $v_p = v_n$
- $A = \infty$ $R_i = \infty$ $R_o = 0$

[Ulaby & Maharbiz]

- The previous analysis was far too messy to give any meaningful insight
- Idealizing the op-amp makes our life much easier, and lest us quickly derive the first order behavior of any op-amp circuit

Example Re-Visited



[Ulaby & Maharbiz]

KCL at node v_n:

$$\frac{v_n - v_o}{R_1} + \frac{v_n}{R_2} = 0$$

$$v_n = v_p = v_s$$

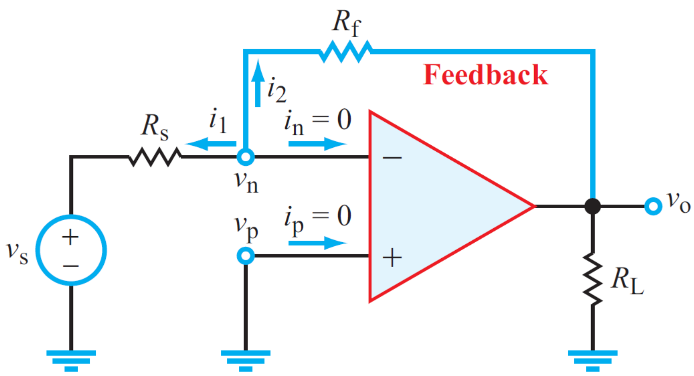
$$v_o = \frac{R_1 + R_2}{R_2} v_s$$

$$G = \frac{v_o}{v_s} = \frac{80k\Omega + 20k\Omega}{20k\Omega} = 5$$

Laundry List of Basic Topologies

- Non-inverting amplifier (previous example)
- Inverting amplifier
- Summing amplifier
- Differencing amplifier
- Unity gain buffer
- Instrumentation amplifier
- Integrator
- Differentiator
- …

Inverting Amplifier



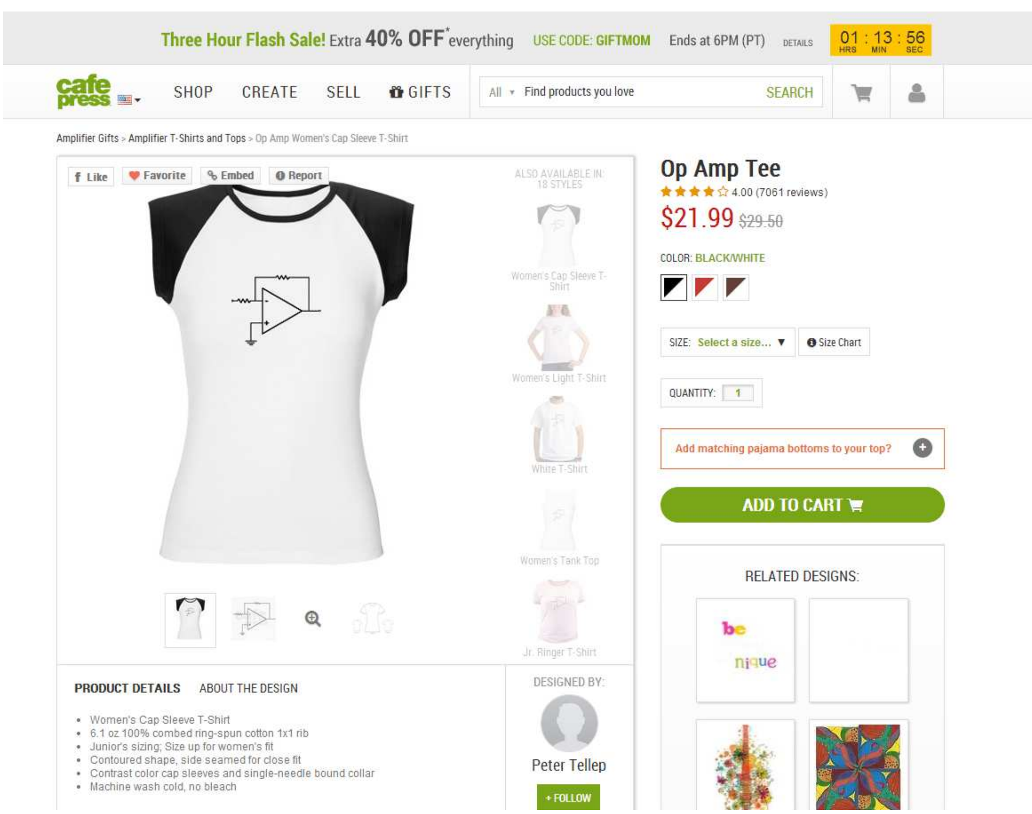
[Ulaby & Maharbiz]

At node v_n

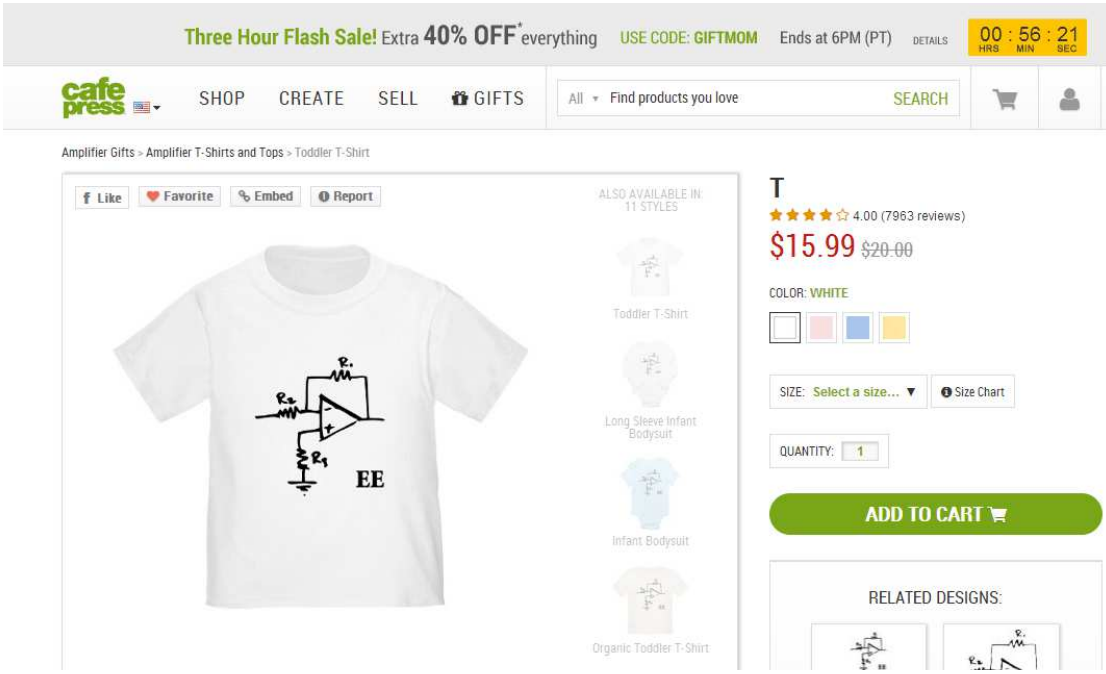
$$\frac{v_n - v_s}{R_s} + \frac{v_n - v_o}{R_f} + i_n = 0.$$

$$v_n = v_p = 0$$

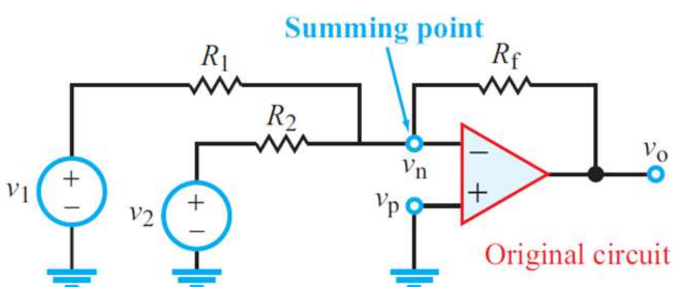
$$G = \frac{v_o}{v_s} = -\left(\frac{R_f}{R_s}\right).$$



Advanced Version!



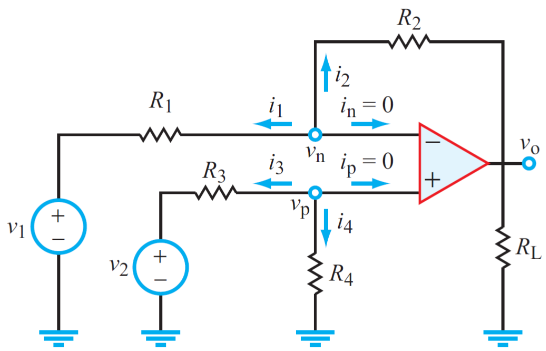
Summing Amplifier (Inverting)



[Ulaby & Maharbiz]

$$v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2\right)$$

Difference Amplifier



[Ulaby & Maharbiz]

At node v_n

$$\frac{v_n - v_1}{R_1} + \frac{v_n - v_o}{R_2} + i_n = 0. \qquad (4.38)$$

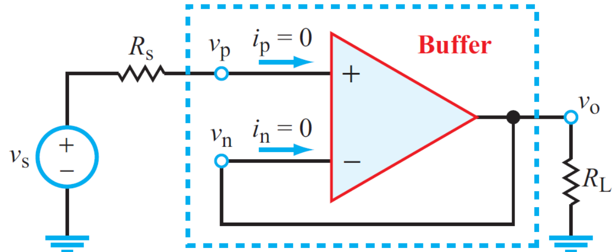
At v_p, $i_3 + i_4 + i_p = 0$, or

$$\frac{v_p - v_2}{R_3} + \frac{v_p}{R_4} + i_p = 0. \qquad (4.39)$$

Upon imposing the ideal op-amp constraints $i_p = i_n = 0$ and $v_p = v_n$, we end up with

$$v_o = \left[\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right] v_2 - \left(\frac{R_2}{R_1}\right) v_1, \qquad (4.40)$$

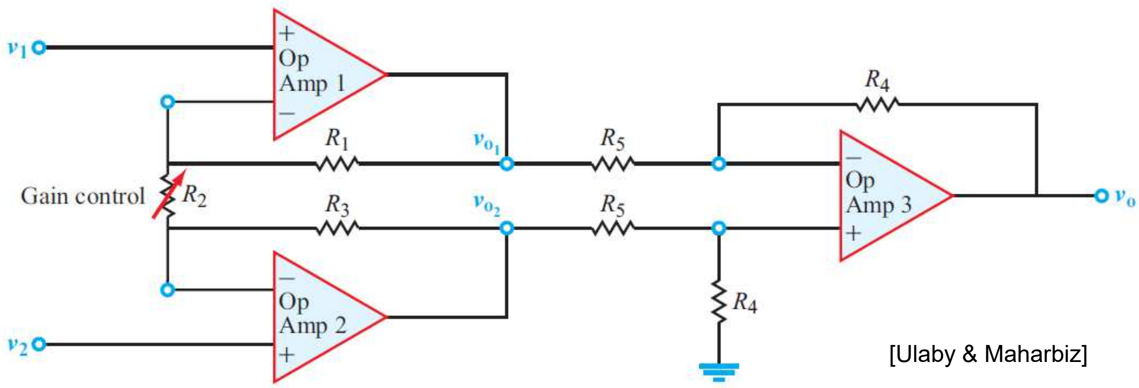
Unity Gain Buffer



[Ulaby & Maharbiz]

$$v_o = v_p = v_s$$

Instrumentation Amplifier



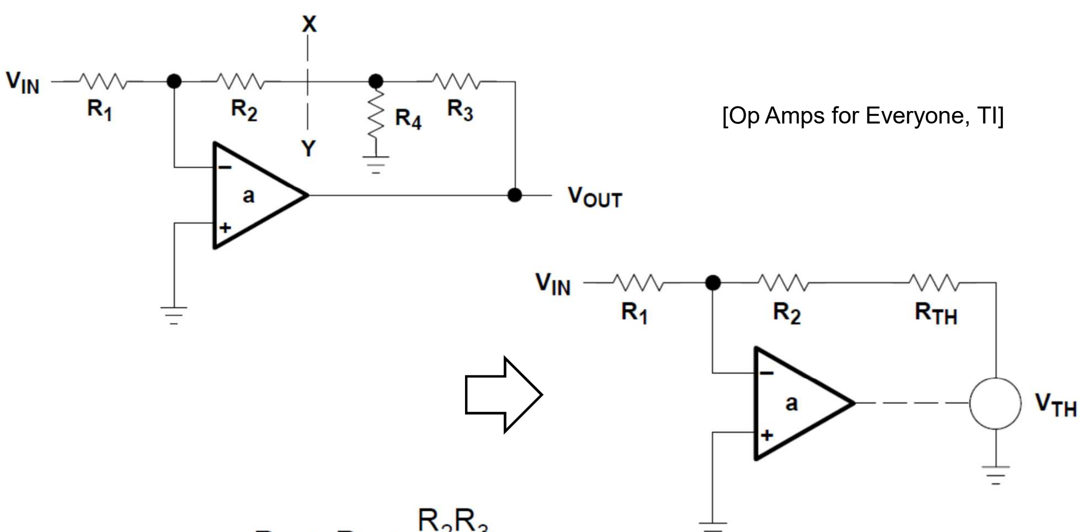
[Ulaby & Maharbiz]

$$v_o = \left(\frac{R_4}{R_5}\right)\left(\frac{R_1+R_2+R_3}{R_2}\right)(v_2 - v_1)$$

If we set $R_1 = R_3 = R_4 = R_5 = R$

$$v_o = \left(1 + \frac{2R}{R_2}\right)(v_2 - v_1).$$

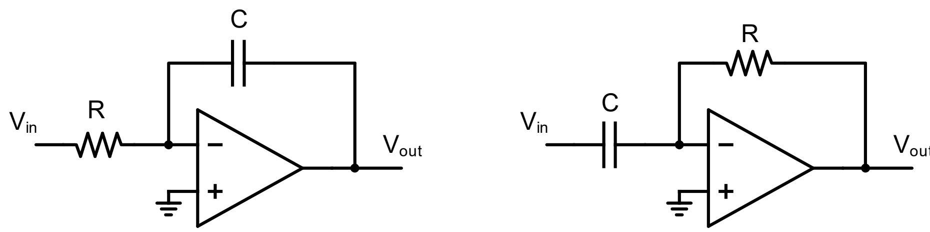
Tricky Feedback Networks



[Op Amps for Everyone, TI]

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_3 + \frac{R_2R_3}{R_4}}{R_1}$$

Integrator and Differentiator

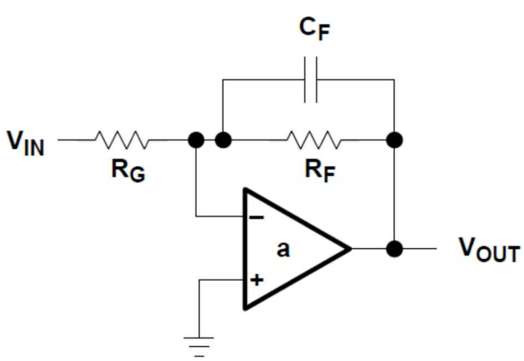


$$\frac{V_{out}}{V_{in}} = -\frac{1}{sRC}$$

$$\frac{V_{out}}{V_{in}} = -sRC$$

- Integrators are a fundamental building block for filters
  - More later

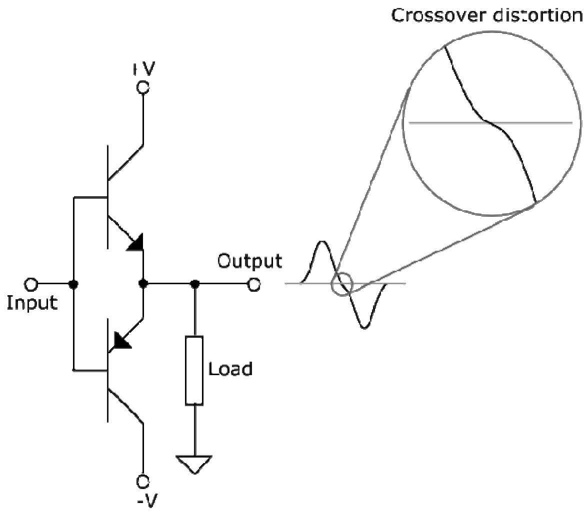
First Order Active Lowpass Filter

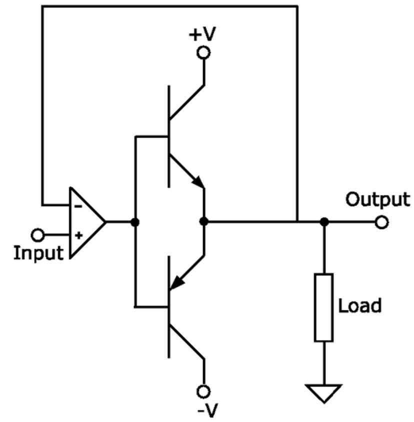


[Op Amps for Everyone, TI]

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{\frac{1}{R_F} + sC_F}}{R_G} = -\frac{R_F}{R_G}\frac{1}{1 + sR_FC_F}$$

Cool Tricks: Eliminating “Crossover Distortion”





http://en.wikipedia.org/wiki/Crossover_distortion

Chapter 13

Feedback Analysis of Opamp Circuits

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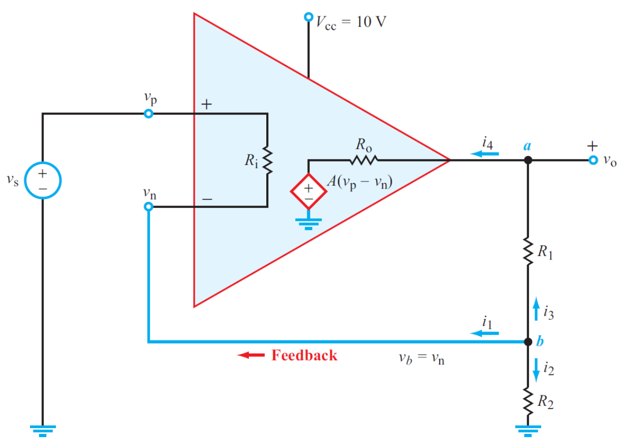
References:
"Op Amps for Everyone" by Texas Instruments, Chapter 6
Maloberti, Chapter 12 (see e-book link under reading material)

Back to Our Example

For $V_{cc} = 10$ V, $A = 10^6$, $R_i = 10^7$ Ω, $R_o = 10$ Ω, $R_1 = 80$ kΩ, and $R_2 = 20$ kΩ,

[Ulaby & Maharbiz]



KCL at Node a:

$$\frac{v_n - v_o}{R_1} = \frac{v_o - A(v_p - v_n)}{R_o}$$

KCL at Node b:

$$\frac{v_n - v_p}{R_i} + \frac{v_n}{R_2} + \frac{v_n - v_o}{R_1} = 0$$

$$G = \frac{v_o}{v_s} = \frac{[AR_i(R_1 + R_2) + R_2R_o]}{AR_2R_i + R_o(R_2 + R_i) + R_1R_2 + R_i(R_1 + R_2)} = 4.999975$$

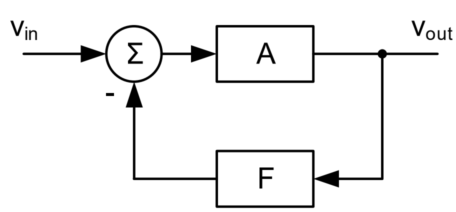
Gain Errror: $\epsilon = \dfrac{4.999975 - 5}{5} = -5 \cdot 10^{-6} = -5\ ppm$

Motivation

- The analysis on the previous page is correct
  - But it is very tedious and does not provide any interesting engineering insight
- In the following treatment, we will look at a more systematic way to analyze the effect of finite gain for this specific example
  - The circuit is interpreted as a feedback system
- Then, we generalize this approach for use in arbitrary opamp feedback circuits

Circuits with Negative Feedback

- First proposed by Harold S. Black, 1927



$$v_{out} = A(v_{in} - Fv_{out})$$

$$A_{CL} = \frac{v_{out}}{v_{in}} = \frac{A}{1+AF} = \frac{1}{F}\frac{T}{1+T}$$

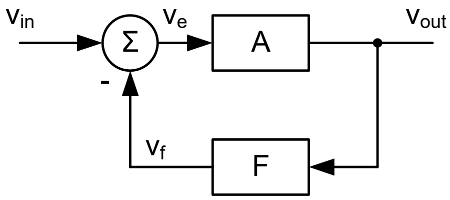
$$T = AF$$

Always a positive quantity for negative feedback

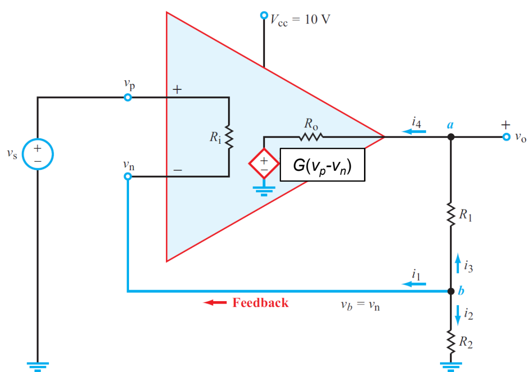
$$A_{CL}\Big|_{T\to\infty} = \frac{1}{F} = A_{CLI}$$

- Key result: When loop gain (T) is large, the closed loop gain (A_{CL}) approaches the ideal closed loop gain (A_{CLI}), which is equal to $1/F$

Identification of A and F



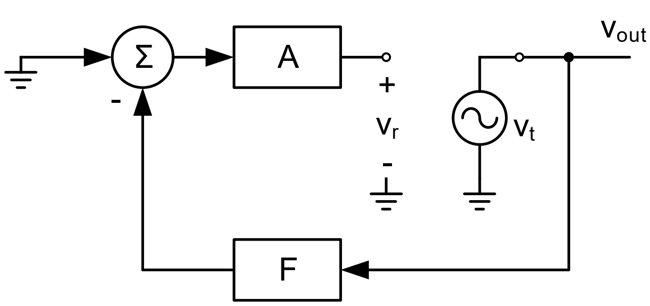
$$F = \frac{v_f}{v_{out}} = \frac{R_2||\cancel{R_i}}{R_2||\cancel{R_i} + R_1} \cong \frac{R_2}{R_2 + R_1}$$



$$A = \frac{v_{out}}{v_n} = G\frac{R_1 + R_2||\cancel{R_i}}{R_1 + R_2||\cancel{R_i} + \cancel{R_o}} \cong G$$

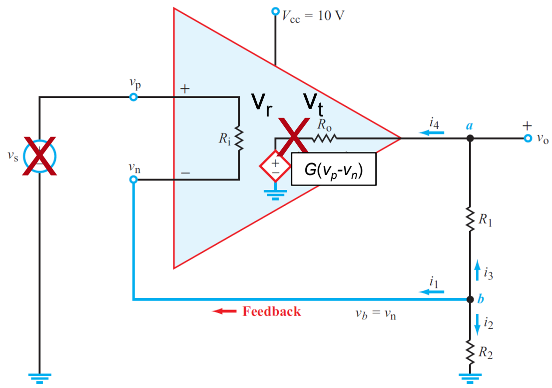
Key point: In typical opamp circuits, R_i and R_o are negligible compared to the resistances used in the feedback network

Better: Think Directly in Terms of Loop Gain



Minus sign due to "-" at summing node

$$T = AF = -\frac{v_r}{v_t}$$



Note: To find the loop gain, it is best to break the loop at the opamp's voltage controlled voltage source.

This approach preserves all of the node impedances in the circuit.

$$T = -\frac{v_r}{v_t} = G\frac{R_2||\cancel{R_i}}{R_2||\cancel{R_i} + R_1 + \cancel{R_o}} \cong 10^6\frac{20k\Omega}{20k\Omega + 80k\Omega} = 200{,}000$$

(Exact value: 199,600, above approximation has 0.2% error)

Closed-Loop Gain Calculation

$$A_{CL} = A_{CLI}\frac{T}{1+T} \cong A_{CLI}\left(1-\frac{1}{T}\right) \qquad \epsilon \cong \frac{A_{CLI}\left(1-\frac{1}{T}\right) - \mathrm{A_{CLI}}}{\mathrm{A_{CLI}}} = -\frac{1}{\mathrm{T}}$$

- Note that we already know A_{CLI} from the ideal opamp analysis
  - Infinite opamp gain automatically implies infinite loop gain

$$A_{CL} = 5 \cdot \frac{200{,}000}{1 + 200{,}000} = 4.999975 \qquad \epsilon \cong \frac{1}{200{,}000} = 5ppm$$

- Same result as before, except that we did not have to go through a painful nodal analysis

What if the Opamp Gain Changes?

$$A_{CL} = 5 \cdot \frac{200{,}000}{1 + 200{,}000} = 4.999975$$

- Cut the gain in half:

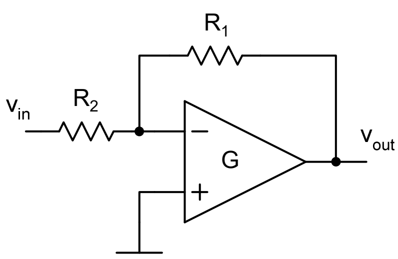
$$A_{CL} = 5 \cdot \frac{100{,}000}{1 + 100{,}000} = 4.999950$$

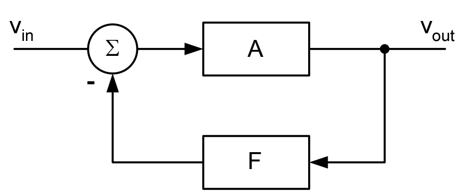
- Double the gain:

$$A_{CL} = 5 \cdot \frac{400{,}000}{1 + 400{,}000} = 4.999988$$

- The closed-loop gain is immune to large variations in opamp gain
- The voltage gain of the overall circuit is primarily defined by the divider ratio of the resistive feedback
  – A quantity that we can control very precisely

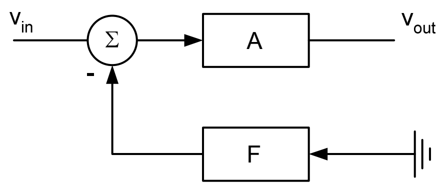
Inverting Configuration



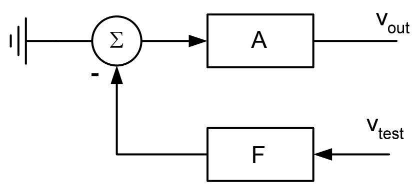


- It is not immediately clear how to map this circuit into the block diagram representation
  – Both resistors affect the input and feedback path
  – Electronic components are not unidirectional, as assumed in the block diagram (which has no notion of impedance)
- We can still try to make this work using superposition…

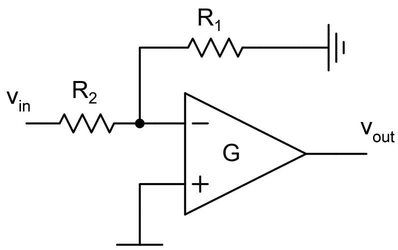
Superposition



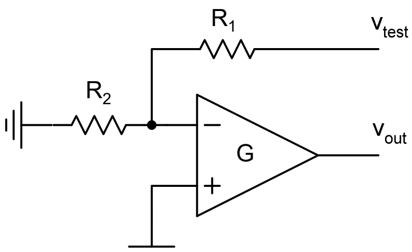
$$\Rightarrow A$$



$$\Rightarrow -AF$$



$$A = -\frac{R_1}{R_1 + R_2} G$$

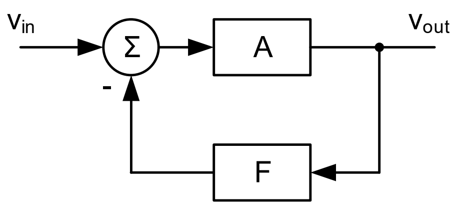


$$-AF = -\frac{R_2}{R_1 + R_2} G$$

(Note: Same loop gain as non-inverting circuit!)

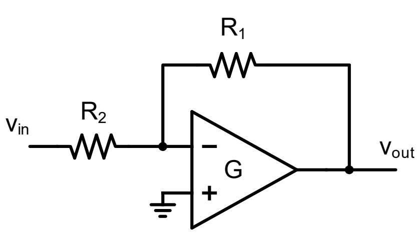
Result

$$A = -\frac{R_1}{R_1 + R_2} G \qquad\qquad F = \frac{AF}{A} = \frac{\frac{R_2}{R_1 + R_2} G}{-\frac{R_1}{R_1 + R_2} G} = -\frac{R_2}{R_1} = \frac{1}{A_{CLI}}$$



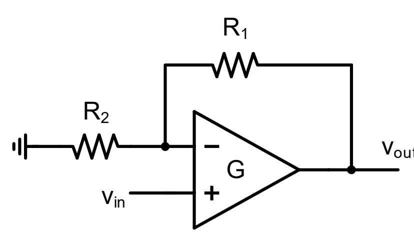
- From the KCL analysis with infinite amplifier gain we already knew A_{CLI}, and this has to be equal to $1/F$ in the assumed representation
- Beyond that, all we need to know is the loop gain to compute the deviation from ideality
  - We do not really need to know what A is…

Comparison



$$T = \frac{R_2}{R_1 + R_2} G$$

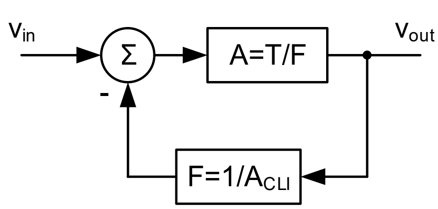
$$A_{CLI} = -\frac{R_1}{R_2}$$



$$T = \frac{R_2}{R_1 + R_2} G$$

$$A_{CLI} = \frac{R_1 + R_2}{R_1}$$

Model valid for both topologies:



Methodology for Opamp Circuit Analysis

- Find A_{CLI} using nodal analysis, assuming infinite opamp gain
  - Often this is done by inspection, or simply by remembering the result
- Find the loop gain to compute the deviation term
  - This is usually straightforward, especially when there are ideal breakpoints that do not alter the impedance loading around the loop
  - The best breakpoint for a voltage amplifier is right at the controlled voltage source (see example on slide 7)
- Done!

$$A_{CL} = \frac{v_{out}}{v_{in}} = A_{CLI}\frac{T}{1+T}$$

Advanced Analysis Frameworks

- Return ratio analysis
  - Proposed by Bode
  - Very similar to the flow we have followed, except that it includes extensions to handle feedforward through the feedback network
    - Relevant when the forward amplifier has high output impedance
    - Not significant in the examples we consider in EE101B
- Two-port analysis
  - Proposed by Black
  - Map the feedback network onto one of four topologies
    - Voltage-voltage, voltage-current, current-voltage, current-current feedback; depending on what the desired input/output quantities are
    - Model the feedback network as an ideal two-port and absorb impedance loading effects into a
  - In my opinion, an overkill for gaining basic intuition about feedback…
  - Have a look at Maloberti, Chapter 12, if you are interested

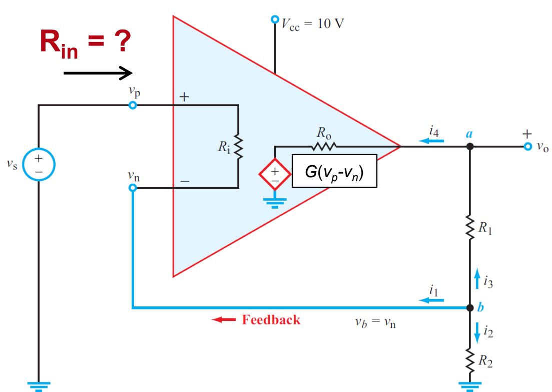
Feedback and Port Impedances

- Feedback not only helps desensitize the circuit to amplifier gain variations, it also lets us control/improve the port impedances
- We can calculate the port impedances of arbitrary feedback circuits using "Blackman's Impedance Formula"
  - Based on loop gain calculations
  - Extremely useful and easy to use

$$Z_{port} = Z_{port0} \cdot \frac{1 + T(port\ shorted)}{1 + T(port\ open)}$$

- Z_{port0} is the port impedance with the loop's gain element set to zero
- $T(port\ shorted)$ is the loop gain with the port under consideration shorted
- $T(port\ open)$ is the loop gain with the port under consideration open

Example: Input Resistance of Non-Inverting Configuration



Intuition: Think Miller effect!

- To find R_{in0} set the amplifier gain to zero

$$R_{in0} \cong R_i$$

- To find $T(port\ shorted)$ we short v_p to ground and find T

$$T(port\ shorted) \cong G\frac{R_2}{R_2 + R_1}$$

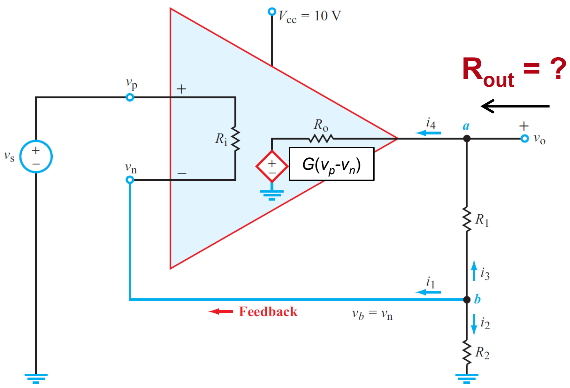
- To find $T(port\ open)$ we leave v_p floating and find T

$$T(port\ open) = 0$$

$$R_{in} = R_i \cdot \frac{1 + G\frac{R_2}{R_2 + R_1}}{1 + 0} \cong R_i \cdot 200{,}000$$

Increased by loop gain → huge

Example: Output Resistance of Non-Inverting Configuration



R_{out} = ?

- To find R_{out0} set the amplifier gain to zero

$$R_{out0} \cong R_o$$

- To find $T(port\ shorted)$ we short v_o to ground and find T

$$T(port\ shorted) = 0$$

- To find $T(port\ open)$ we leave v_o open and find T

$$T(port\ open) \cong G\frac{R_2}{R_2 + R_1}$$

$$R_{out} = R_o \cdot \frac{1+0}{1 + G\dfrac{R_2}{R_2+R_1}} \cong \frac{R_o}{200{,}000}$$

Decreased by loop gain → tiny

Chapter 14

Frequency Response of Opamp Circuits

Boris Murmann

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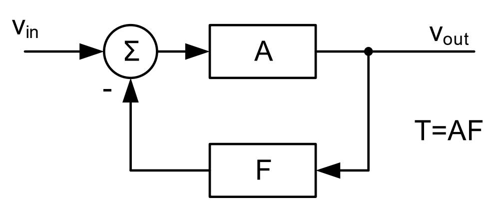
References:
"Op Amps for Everyone" by Texas Instruments, Chapter 6
Maloberti, Chapter 12 (see e-book link under reading material)

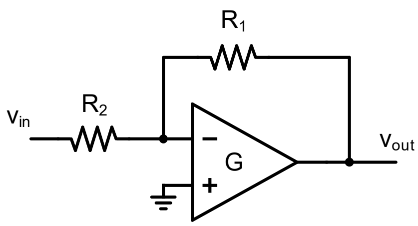
Opamp Feedback Circuit Model

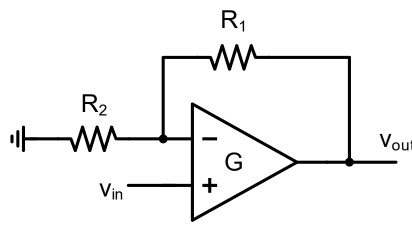


- Find F by analyzing the circuit with an infinite gain opamp. This yields $F = 1/A_{CLI}$, where A_{CLI} is the ideal closed-loop gain.
- Find the loop gain T by injecting a test signal at a suitable breakpoint. $T = -v_r/v_t$, the ratio between return voltage and injected test voltage.
- The closed loop behavior is fully defined once F and T are known. We often do not care what A is, but we can compute it using $A = T/F$.

$$A_{CL} = \frac{v_{out}}{v_{in}} = \frac{1}{F}\frac{T}{1+T} = \frac{A}{1+T}$$

Basic Examples





$$A_{CLI} = -\frac{R_1}{R_2}$$

$$A_{CLI} = \frac{R_1 + R_2}{R_2}$$

$$T = \frac{R_2}{R_1 + R_2} G$$

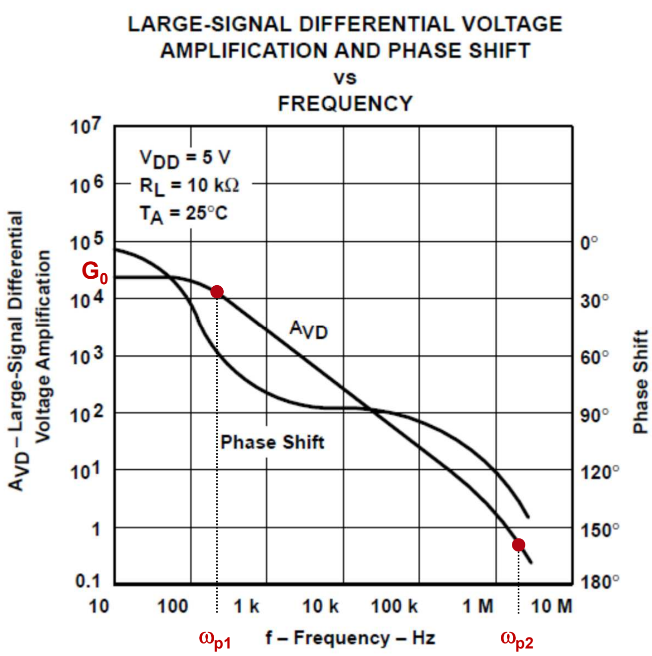
(same!)

$$T = \frac{R_2}{R_1 + R_2} G$$

$$A = TA_{CLI} = -\frac{R_1}{R_1 + R_2} G$$

$$A = TA_{CLI} = G$$

Frequency Response of a TLC272 Opamp



- At first glance, this amplifier seems to have two LHP poles
  - One at low frequencies
  - One at high frequencies

$$G(s) = \frac{G_0}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)}$$

- Let's start by modeling only the dominant pole (at low frequencies)

Loop Gain

- For both of the above circuit examples, we now have

$$T(s)=\frac{R_2}{R_1+R_2}G(s)=\frac{R_2}{R_1+R_2}\frac{G_0}{\left(1-\frac{s}{p_1}\right)}$$

$$T(s)=\frac{T_0}{\left(1-\frac{s}{p_1}\right)}$$

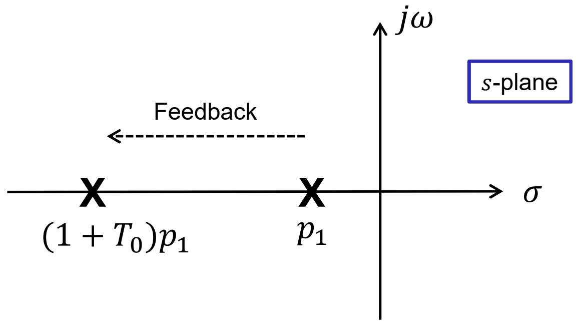
- T_0 is the DC loop gain

Closed Loop Gain

$$A_{CL}(s)=\frac{1}{F}\frac{T(s)}{1+T(s)}=\frac{1}{F}\frac{\frac{T_0}{\left(1-\frac{s}{p_1}\right)}}{1+\frac{T_0}{\left(1-\frac{s}{p_1}\right)}}=\frac{1}{F}\frac{T_0}{\left(1-\frac{s}{p_1}\right)+T_0}$$

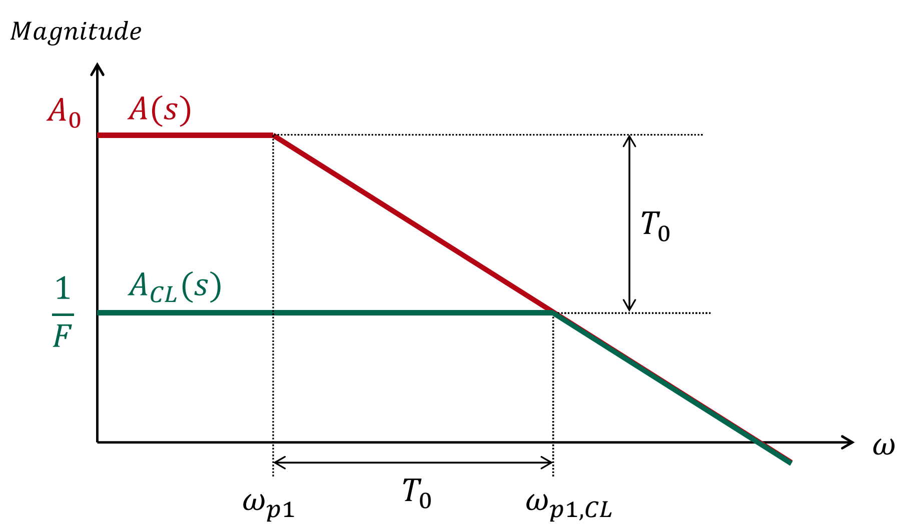
$$A_{CL}(s)=\frac{1}{F}\frac{T_0}{1+T_0}\frac{1}{\left(1-\frac{s}{p_1(1+T_0)}\right)}=\frac{A_0}{\boldsymbol{1+T_0}}\frac{1}{\left(1-\frac{s}{p_1(\boldsymbol{1+T_0})}\right)}$$

$$For\ T_0\gg 1\qquad A_{CL}(s)\cong\frac{1}{F}\frac{1}{\left(1-\frac{s}{p_1T_0}\right)}$$

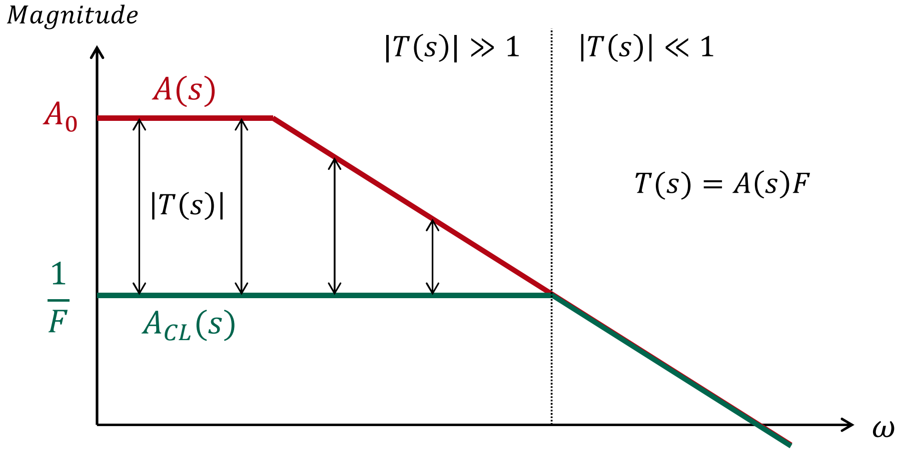


- Applying feedback has increased the bandwidth by $(1+T_0)$
- But, we have sacrificed gain in the process, since $A_{CL0} = A_0/(1+T_0)$
- Essentially, we have traded gain for bandwidth
- Also note that the circuit is stable, since the pole remains in the LHP

Bode Plot (Assuming $T_0 >> 1$)

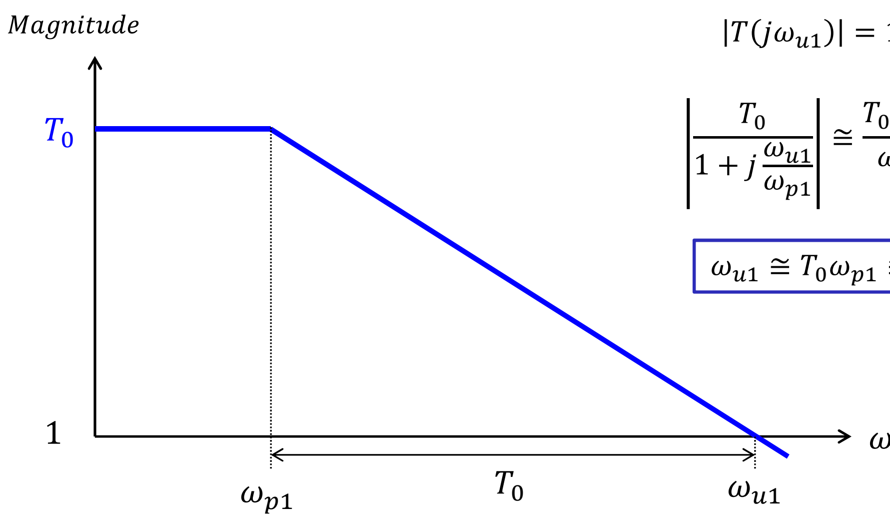


$$A_{CL}(s) = \frac{1}{F}\frac{T(s)}{1+T(s)} = \frac{A(s)}{1+T(s)} \cong \begin{cases} 1/F & for\ |T(s)| \gg 1 \\ A(s) & for\ |T(s)| \ll 1 \end{cases}$$



- The loop forces A_{CL} to be close to $1/F$ until it runs out of loop gain
  - This is where the closed loop pole appears

Bode Plot of Loop Gain



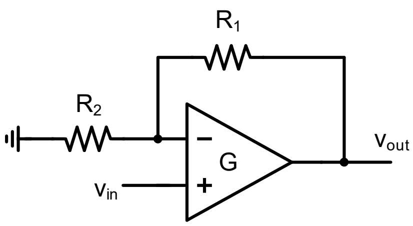
$$|T(j\omega_{u1})| = 1$$

$$\left|\frac{T_0}{1+j\dfrac{\omega_{u1}}{\omega_{p1}}}\right| \cong \frac{T_0\omega_{p1}}{\omega_{u1}} = 1$$

$$\boxed{\omega_{u1} \cong T_0\omega_{p1} \cong \omega_{p1,CL}}$$

- The frequency ω_{u1} is called the unity gain frequency of the loop or loop gain-bandwidth product; it is approximately equal to the closed-loop bandwidth

Example (Non-Inverting Amplifier)

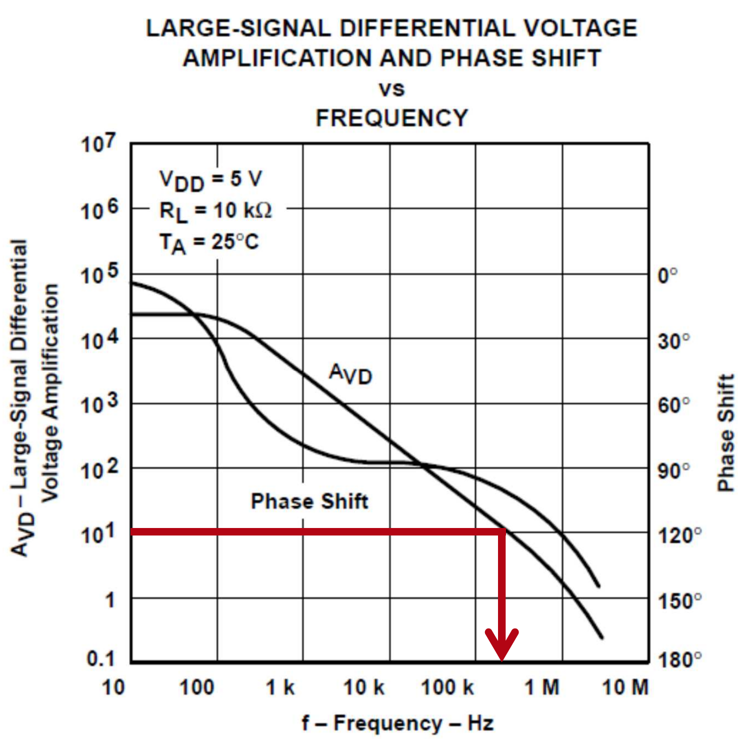


$$A_{CLI} = \frac{R_1 + R_2}{R_2} = 10$$

$$T(s) = \frac{R_2}{R_1 + R_2} G(s) = 0.1G(s)$$

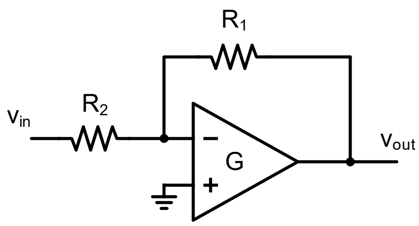
$$|T(s)| = 1 \quad \Rightarrow \quad |G(s)| = 10$$

- The closed-loop bandwidth corresponds to the frequency where the opamp's gain magnitude has reduced to 10.



$\omega_{p1,CL} \cong 200kHz$

Example (Inverting Amplifier)



$$A_{CLI} = -\frac{R_1}{R_2} = -10$$

$$T(s) = \frac{R_2}{R_1 + R_2} G(s) = \frac{1}{11} G(s)$$

$$|T(s)| = 1 \quad \Rightarrow \quad |G(s)| = 11$$

- The closed loop bandwidth corresponds to the frequency where the opamp's gain magnitude has reduced to 11
  - Very close to what we had before, with slightly less bandwidth

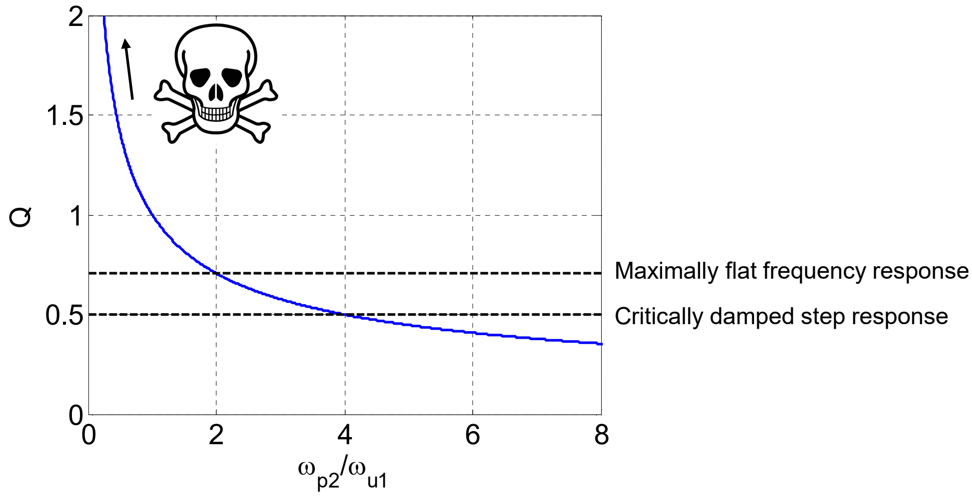
Let's Now Consider the Second Opamp Pole

$$T(s) = \frac{T_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

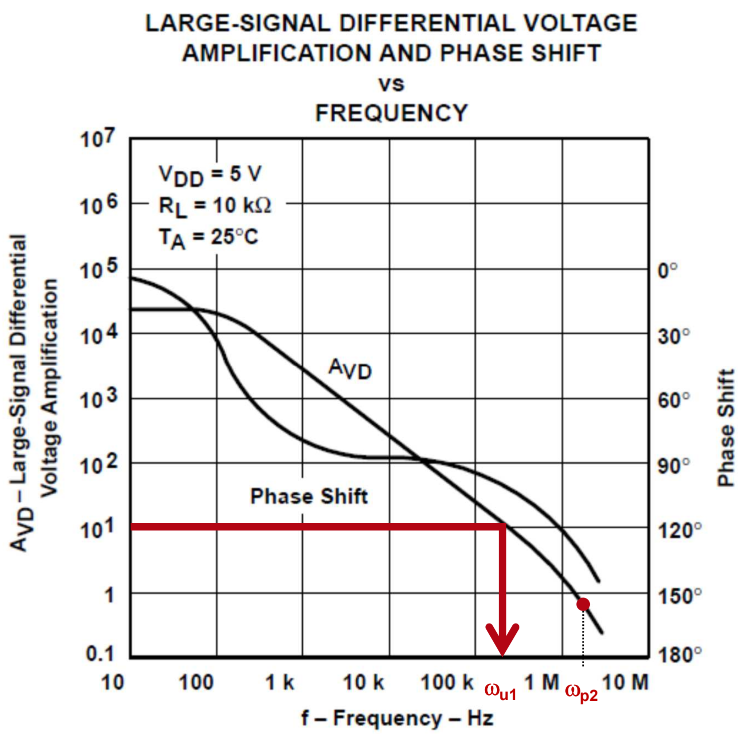
$$A_{CL}(s) = \frac{1}{F} \frac{T(s)}{1 + T(s)} = \frac{1}{F} \frac{T_0}{1 + T_0} \cdot \frac{1}{1 + \frac{\omega_{p1} + \omega_{p2}}{(1 + T_0)\omega_{p1}\omega_{p2}} s + \frac{1}{(1 + T_0)\omega_{p1}\omega_{p2}} s^2}$$

$$A_{CL}(s) = \frac{A_{CL0}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \sqrt{(1 + T_0)\omega_{p1}\omega_{p2}} \cong \sqrt{\omega_{u1}\omega_{p2}} \qquad Q = \frac{\sqrt{(1 + T_0)\omega_{p1}\omega_{p2}}}{\cancel{\omega_{p1}} + \omega_{p2}} \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}}$$



- Key point: In a practical amplifier design, the second pole must occur beyond the loop's unity gain frequency

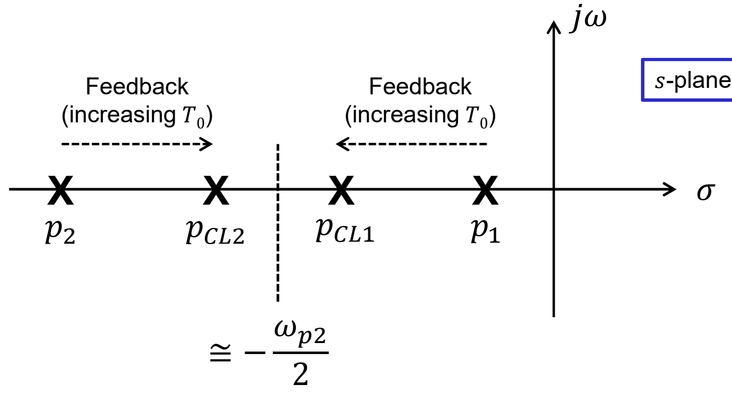


$$Q \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}} \cong \sqrt{\frac{1}{10}} = 0.316$$

- Looks like we're OK with our example circuit
- Open questions
  - What are the locations of the closed-loop poles?
  - What is the exact closed-loop 3-dB bandwidth?

Closed-Loop Pole Positions ($Q \le 0.5$)

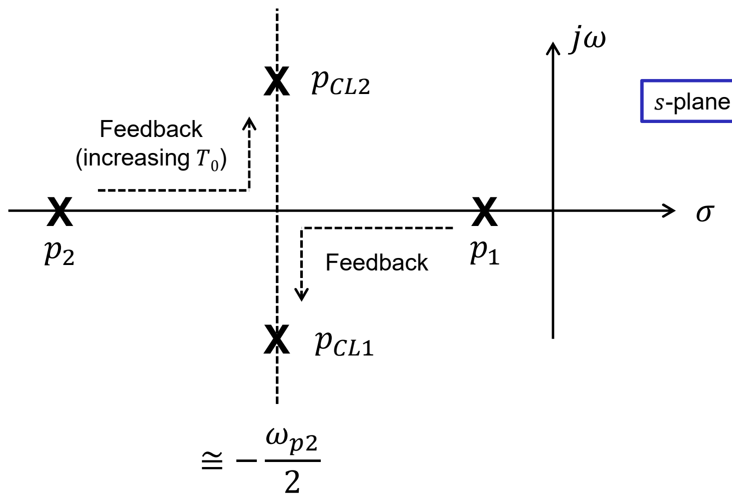
$$p_{CL1,2} = -\frac{\omega_0}{2Q}\left(1 \pm \sqrt{1-4Q^2}\right) \qquad -\frac{\omega_0}{2Q} = -\frac{\omega_{p1}+\omega_{p2}}{2} \cong -\frac{\omega_{p2}}{2}$$



- For $Q = 0.5$ (critically damped step response), the closed loop circuit has two coincident real poles at approximately $p_2/2$

Closed-Loop Pole Positions ($Q > 0.5$)

$$p_{CL1,2} = -\frac{\omega_0}{2Q}\left(1 \pm j\sqrt{4Q^2-1}\right) \qquad -\frac{\omega_0}{2Q} = -\frac{\omega_{p1}+\omega_{p2}}{2} \cong -\frac{\omega_{p2}}{2}$$



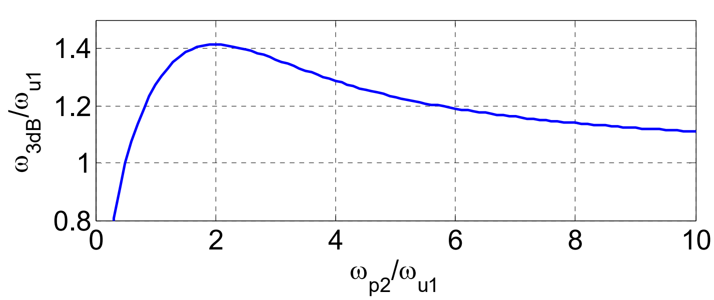
Exact Closed-Loop 3-dB Frequency

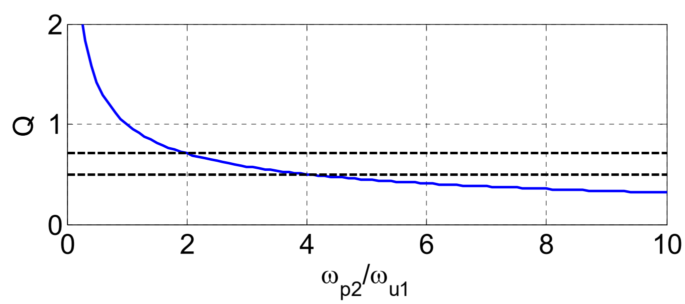
$$A_{CL}(s) = \frac{A_{CL0}}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \cong \frac{A_{CL0}}{1+\frac{s}{\omega_{u1}}+\frac{s^2}{\omega_{u1}\omega_{p2}}} \qquad \omega_0 \cong \sqrt{\omega_{u1}\omega_{p2}} \quad Q \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}}$$

- Note that for $\omega_{p2} \to \infty$, the closed loop response approaches the expression we derived for a single pole feedback system
- To find the 3-dB bandwidth we need to solve this equation:

$$\left|\frac{1}{1+j\frac{\omega_{3dB}}{\omega_{u1}}-\frac{\omega_{3dB}^2}{\omega_{u1}\omega_{p2}}}\right| = \frac{1}{\sqrt{2}}$$

- Best done numerically…





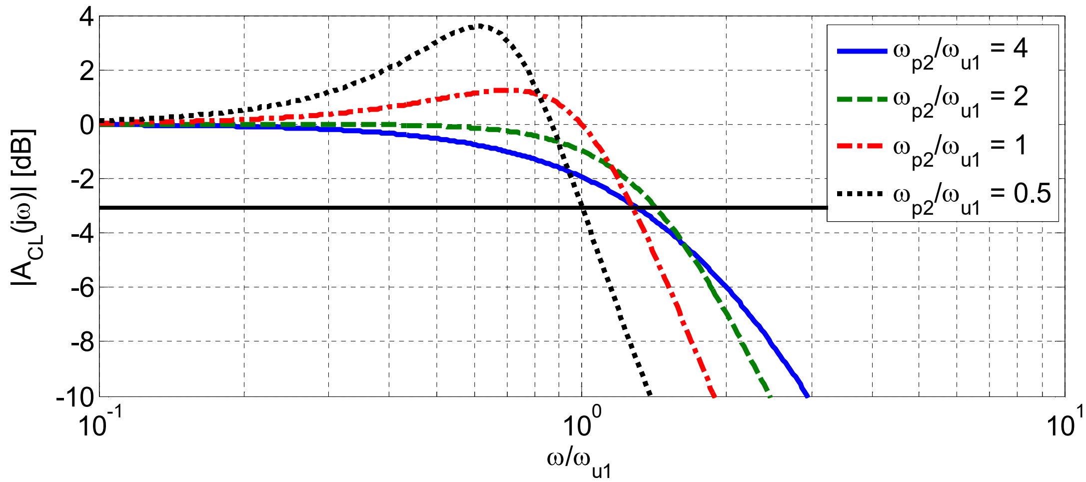
- As expected, for large ω_{p2}/ω_{u1}, the bandwidth approaches that of a first order system (ω_{u1})
- The bandwidth is maximum for the maximally flat response:

$$Q = \frac{1}{\sqrt{2}} \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}}$$

$$\omega_{p2} = 2\omega_{u1}$$

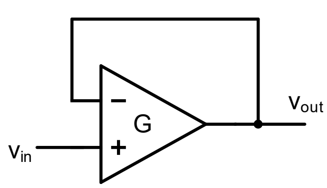
$$\omega_{3dB} = \omega_0 \cong \sqrt{\omega_{u1}\omega_{p2}}$$

$$\boxed{\omega_{3dB} \cong \omega_{u1}\sqrt{2}}$$



- Bottom line
  - If possible, design for a maximally flat response ($\omega_{p2} = 2\omega_{u1}$)
  - Pushing ω_{p2} to higher frequencies is also fine (not much loss in BW)
  - Definitely avoid placing the second pole close to or before ω_{u1}
    - Peaking, bandwidth loss and significant step response ringing

Unity Gain Configuration

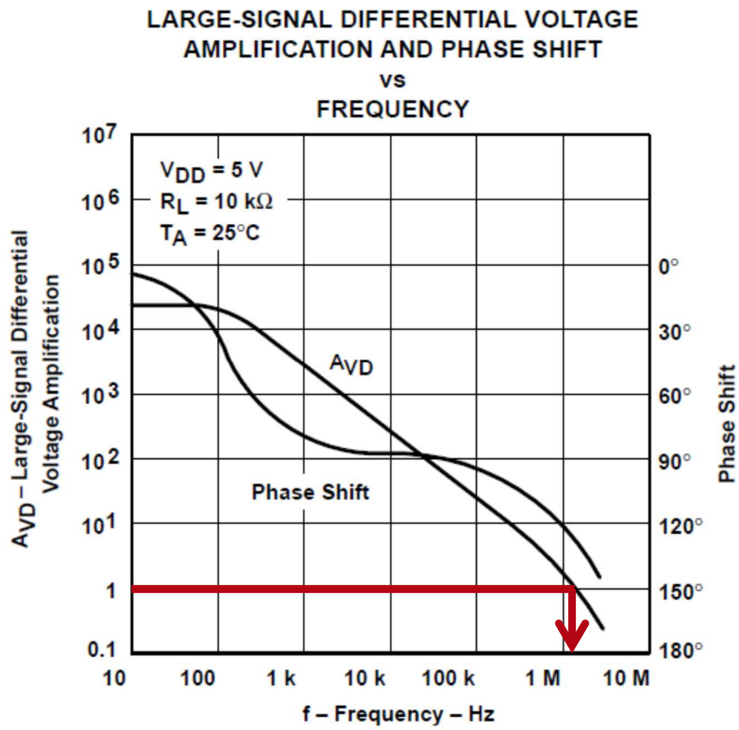


$$A_{CLI} = 1$$

$$T(s) = G(s)$$

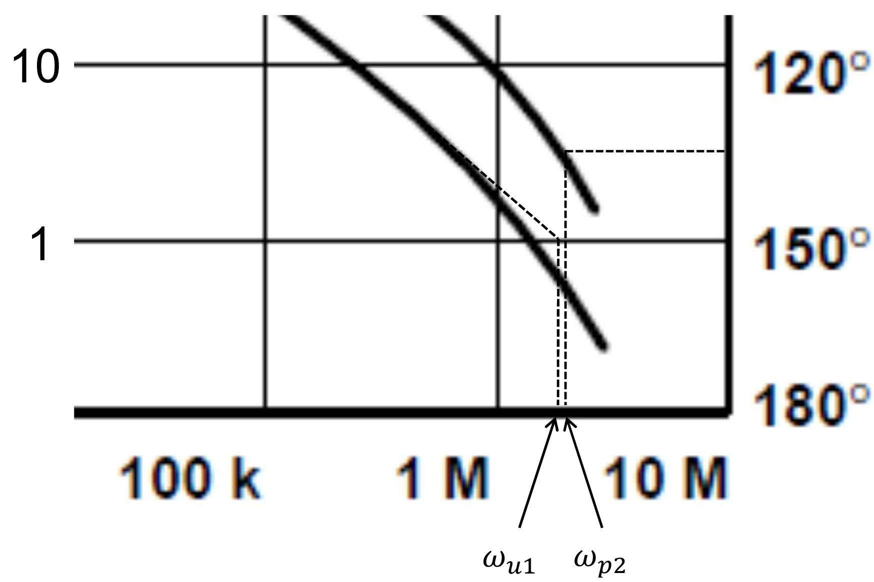
$$|T(s)| = 1 \quad \Rightarrow \quad |G(s)| = 1$$

- The closed loop bandwidth corresponds to the frequency where the opamp's gain magnitude has reduced to unity → larger bandwidth and larger ω_{u1} than in the previous example



- Looks like we may be in trouble
- The second pole is now close to the loop's unity gain frequency

Zoom



$$\omega_{p2} \cong \omega_{u1} \qquad\qquad Q \cong 1$$

Discussion

- This opamp was skillfully designed so that in the worst case (unity gain configuration) it still achieves a reasonable frequency and step response
- This is usually the case for “internally compensated” opamps
  - We will cover the concept of frequency compensation next

- Question: Should the vendor of this part consider reducing ω_{u1} so that there is more “margin” and potentially less peaking/ringing when the opamp is used as a unity gain buffer?

Chapter 15

Stability of Opamp Circuits

Boris Murmann

Stanford University

References:
"Op Amps for Everyone" by Texas Instruments, Chapter 7
Maloberti, Chapter 12 (see e-book link under reading material)

Motivation

- We studied the frequency response of opamps with one and two poles
  - In both cases, the circuit is still stable with feedback applied, i.e. the poles can never wander into the right half plane
- However, in the circuit with two poles we must make one of the poles dominant to "tame" the Q of the closed-loop transfer function
  - The second pole should occur at least 2-4x beyond the extrapolated loop unity gain frequency (ω_{u1})
- Unfortunately, many practical opamp circuits will have more than two poles (and also unwanted zeros) in their loop transfer function, and this can lead to an unstable system
- Let's have a look at a simple example with three poles

Three-Pole Example

- Consider a circuit with three identical poles in its loop gain, and a feedback network with a constant transfer function F

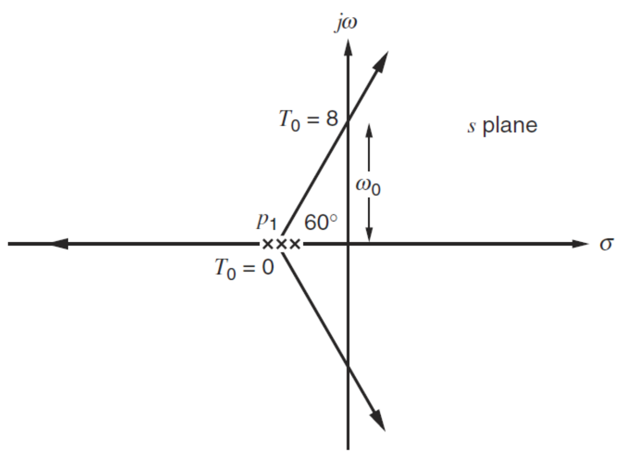
$$T(s) = A(s)F = \frac{T_0}{\left(1-\frac{s}{p_1}\right)^3} \qquad A_{CL}(s) = \frac{1}{F}\frac{T(s)}{1+T(s)} = \frac{1}{F}\frac{\frac{T_0}{\left(1-\frac{s}{p_1}\right)^3}}{1+\frac{T_0}{\left(1-\frac{s}{p_1}\right)^3}} = \frac{1}{F}\frac{T_0}{\left(1-\frac{s}{p_1}\right)^3+T_0}$$

- The poles of $A_{CL}(s)$ are therefore the solution to

$$\left(1-\frac{s}{p_1}\right)^3 + T_0 = 0 \qquad \left(1-\frac{s}{p_1}\right)^3 = -T_0$$

$$\left(1-\frac{s}{p_1}\right) = \sqrt[3]{-T_0} = -\sqrt[3]{T_0} \quad \text{or} \quad \left(1-\frac{s}{p_1}\right) = \sqrt[3]{T_0}e^{j60°} \quad \text{or} \quad \left(1-\frac{s}{p_1}\right) = \sqrt[3]{T_0}e^{-j60°}$$

$$s_1 = p_1\left(1+\sqrt[3]{T_0}\right)$$
$$s_2 = p_1\left(1-\sqrt[3]{T_0}e^{j60°}\right)$$
$$s_3 = p_1\left(1-\sqrt[3]{T_0}e^{-j60°}\right)$$



$$0 = 1-\mathrm{Re}\left(\sqrt[3]{T_0}e^{j60°}\right)$$
$$0 = 1-\sqrt[3]{T_0}\cos(60°)$$
$$\Rightarrow T_0 = 8$$

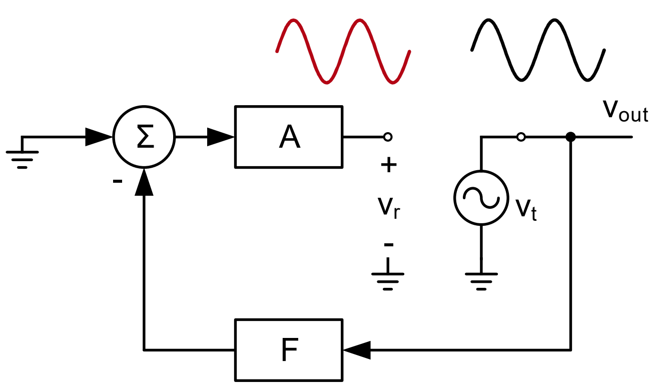
- Conclusion: A feedback amplifier with three identical poles is unstable unless we limit the low-frequency loop gain to less than eight!

Stability

- What we already know
  - The most general stability criterion is BIBO
  - An LTI system is stable if all of its poles are in the LHP
- Since the circuits we consider are LTI, we could (in principle) always compute the closed-loop poles to check stability
  - But this is very tedious, especially for systems with more than 2 poles
- Assuming that the system before closing the loop is stable, we can use a simplified approach, called the "Bode Criterion"

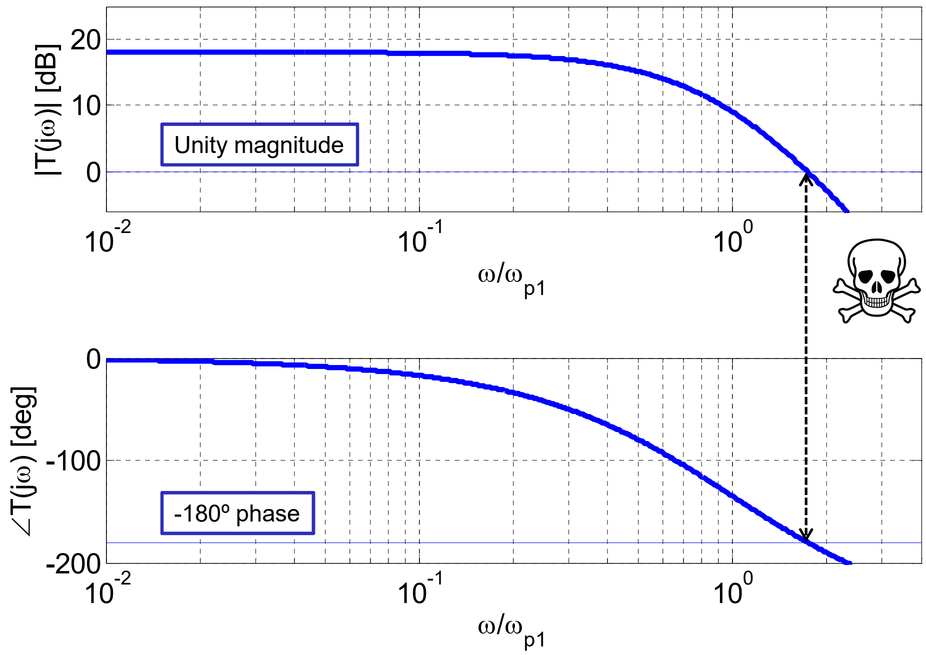
A closed-loop system is stable if the open-loop system is stable and the frequency response of the loop gain has a magnitude of less than unity at the frequency where its phase shift is -180°

Intuition

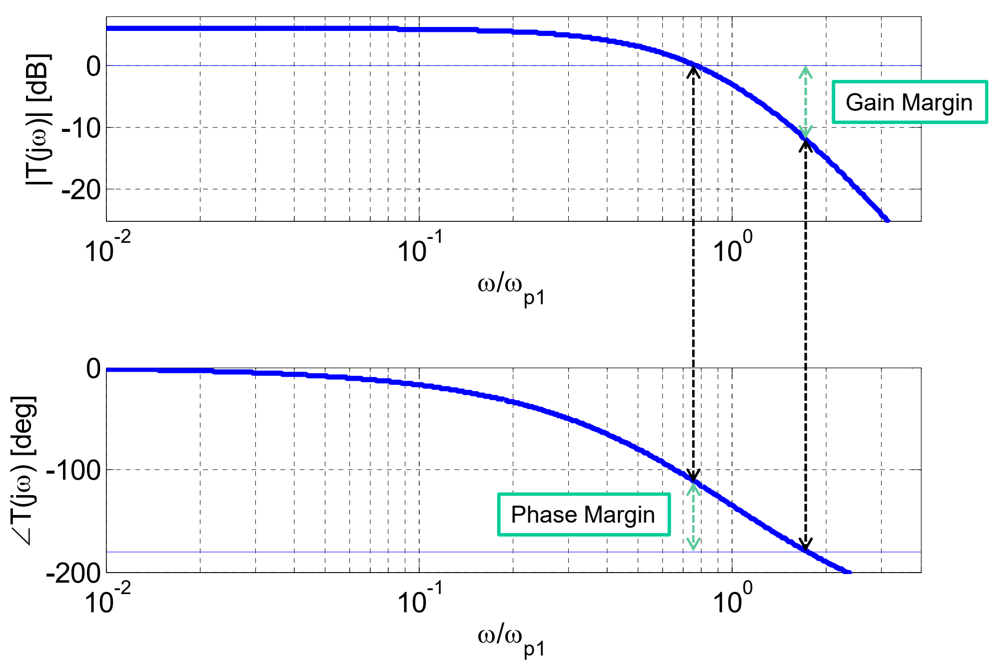


- Suppose we inject a sinusoid into a circuit that has a loop gain magnitude of 1 and a phase shift of -180º at the sinusoid's frequency
- Together with the minus sign at the summing node, the original signal v_t with the same amplitude and phase will return at v_r
- We can close the loop and it will then sustain an everlasting oscillation, even with v_t removed → This is indicative of closed-loop poles on the $j\omega$ axis

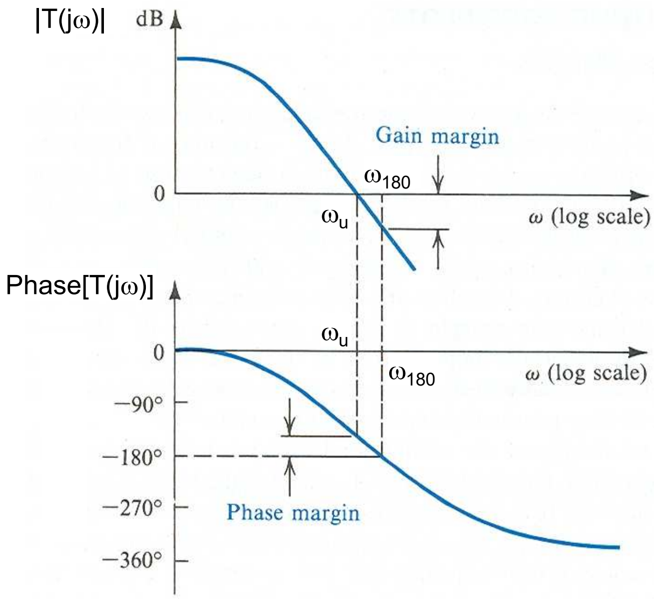
Bode Plot of $T(s)$ for Three-Pole Example ($T_0 = 8$)



Bode Plot of $T(s)$ for Three-Pole Example ($T_0 = 2$)



Definition of Stability Margins



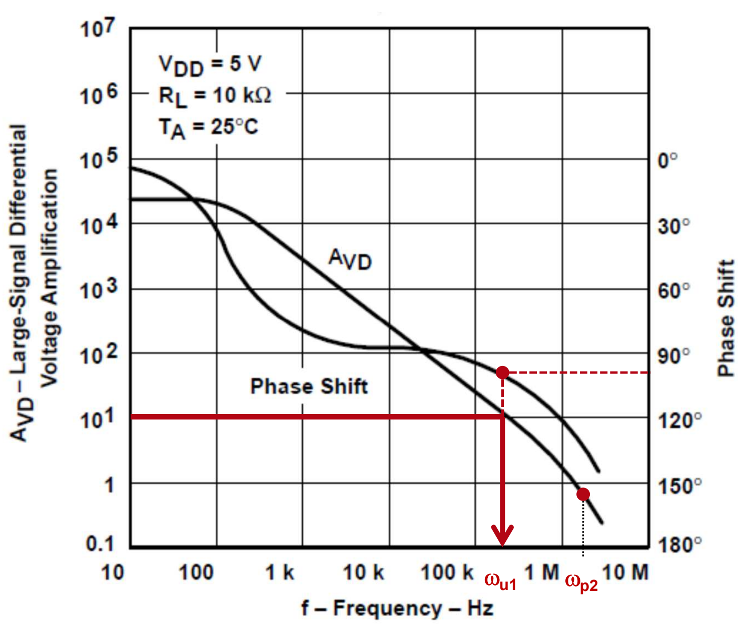
$$GM = \frac{1}{|T(j\omega)|}\bigg|_{\omega=\omega 180}$$

Typically want GM ≥ 3…5

$$PM = 180° + Phase[T(j\omega)]_{\omega=\omega_u}$$

Typically want PM ≥ 60…70°

Another Look At Our TLC272 Example (A_{CLI}=10)



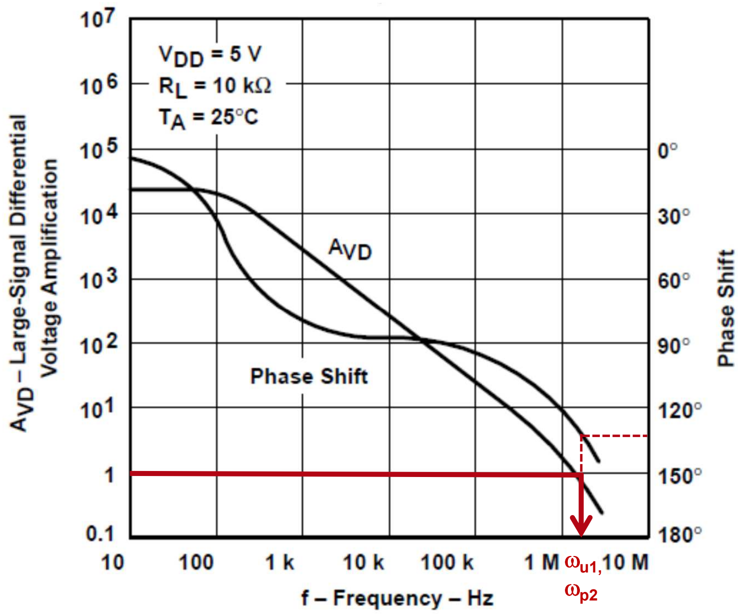
$$\omega_{p1,CL} \cong 200kHz$$

$$Q \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}} \cong \sqrt{\frac{1}{10}} = 0.316$$

$$PM \cong 180° - 100° = 80°$$

Large phase margin ↔ Low Q

Another Look At Our TLC272 Example (A_{CLI}=1)



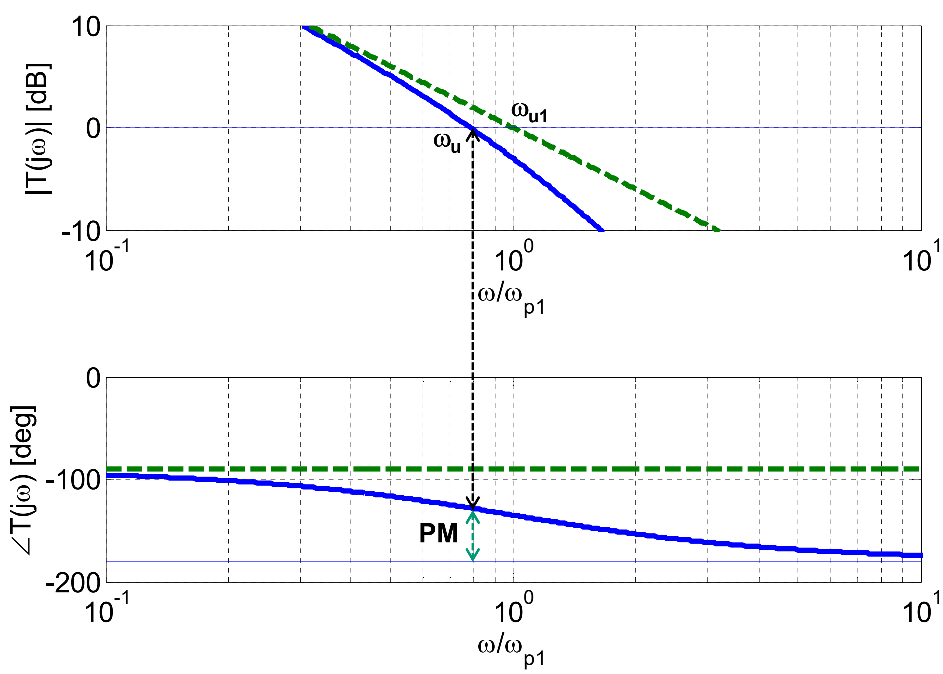
$$\omega_{p1,CL} \cong 2MHz$$

$$Q \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}} \cong 1$$

$$PM \cong 180° - 135° = 45°$$

Small phase margin ↔ High Q

Detailed View of Second Order Crossover



Relationship Between Parameters

- We can find the relationship between ω_u and ω_{u1} using

$$\left|\frac{T_0}{\left(1+\frac{j\omega_u}{\omega_{p1}}\right)\left(1+\frac{j\omega_u}{\omega_{p2}}\right)}\right| \cong \left|\frac{\omega_{u1}}{j\omega_u\left(1+\frac{j\omega_u}{\omega_{p2}}\right)}\right| = 1$$

$$\Rightarrow \left(\frac{\omega_{u1}}{\omega_u}\right)^2 = \frac{1}{2} + \sqrt{\frac{1}{4} + \left(\frac{\omega_{u1}}{\omega_{p2}}\right)^2}$$

- Once we know ω_u, we can easily compute the phase margin

$$PM = 180° - 90° - \arctan\left(\frac{\omega_u}{\omega_{p2}}\right)$$

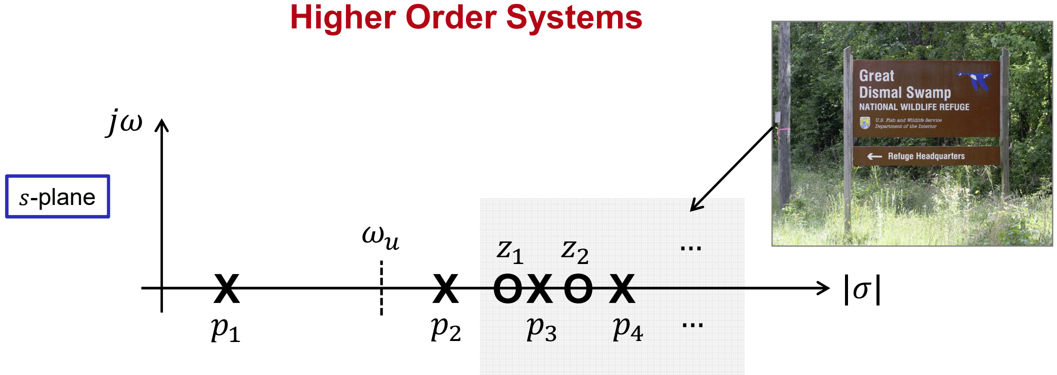
Resulting Relationship Between Phase Margin and Q

$$Q \cong \sqrt{\frac{\omega_{u1}}{\omega_{p2}}}$$

ω_{p2}/ω_{u1}	Q	ω_u/ω_{u1}	PM (º)	ω_{3dB}/ω_{u1}
1	1	0.786	51.8	1.27
2	0.707	0.910	65.5	1.41
4	0.5	0.972	76.3	1.28
10	0.316	0.995	84.3	1.11
∞	—	1	90	1

- Well-designed second order systems have phase margins between 65 and 76 degrees (or higher)

Higher Order Systems



- The majority of practical opamp circuits have a dominant pole and a non-dominant pole past the loop's unity gain frequency
- In addition, there are usually several poles (LHP) and zeros (LHP and RHP) beyond the second pole (inside the opamp, board parasitics, etc.)
- Despite these extra poles/zeros, we can usually still approximate the system as second order
  – The extra poles/zeros mainly affect the phase margin and don't have much bearing on ω_u

$$T(s)=\frac{T_0}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}\frac{\left(1-\frac{s}{z_1}\right)\left(1-\frac{s}{z_2}\right)\ldots\left(1-\frac{s}{z_m}\right)}{\left(1-\frac{s}{p_3}\right)\ldots\left(1-\frac{s}{p_n}\right)}$$

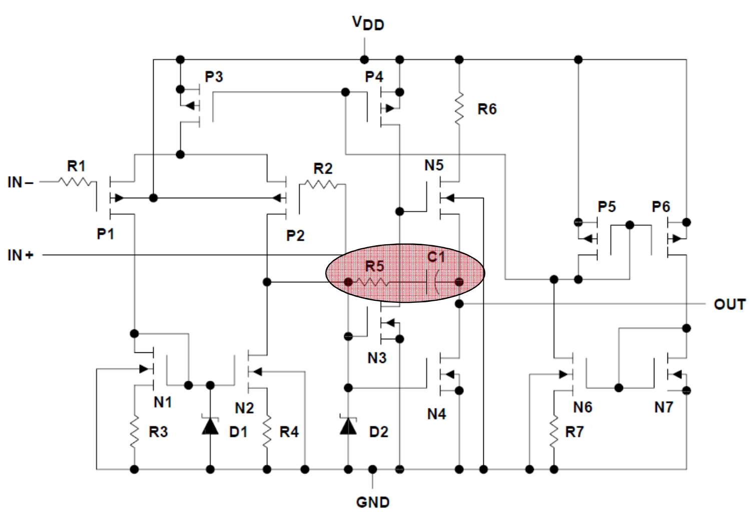
$$T(j\omega)\cong\frac{T_0}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2eq}}\right)}$$

- The equivalent non-dominant pole frequency is given by the frequency at which the overall phase shift of the loop (with all poles and zeros included) is -135º
- This approximation is particularly convenient for interpreting circuit simulation results
- Some rules of thumb
  – A LHP pole or RHP zero 10x past ω_u steals about 5.5º of PM
  – A LHP pole or RHP zero 5x past ω_u steals about 11º of PM

Frequency Compensation

- Frequency compensation refers to the means by which the frequency response of the loop gain is altered to ensure adequate phase margin
- Frequency compensation schemes can be categorized into three groups
  - Internal compensation
    - Alter the frequency response of the opamp
  - External compensation
    - Alter the frequency response of the feedback network
  - Or alter both!
- Our example opamp (TLC272) is internally compensated to ensure reasonable phase margin in the worst case (unity gain feedback)
- In some cases, we may still want to add external compensation to improve the phase margin
  - We'll look at two examples, many more scenarios/options exist
  - See chapter 7 of "Opamps for Everyone"

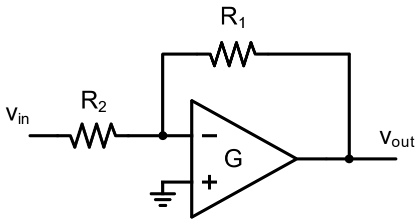
TLC272 Schematic

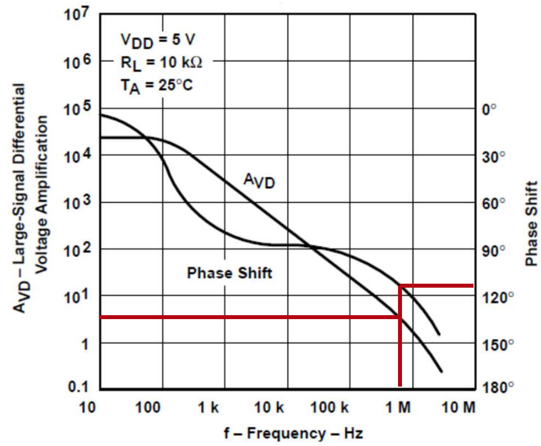


- C_1 and R_5 take care of the opamp's internal frequency compensation
  - These components are sized such that the opamp has a dominant pole and a non-dominant pole beyond unity crossover
  - This is studied in detail in EE114

Motivation for External Compensation

- Say we want to design an inverting amplifier with a gain of -2 using the TLC 272, and we want to have a step response with no overshoot





$$A_{CLI} = -\frac{R_1}{R_2} = -2$$

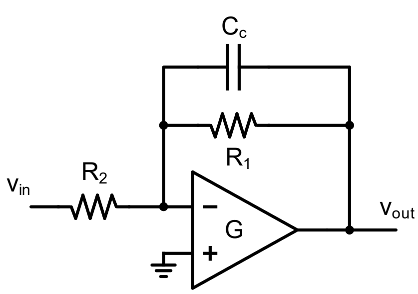
$$T(s) = \frac{R_2}{R_1 + R_2} G(s) = \frac{1}{3} G(s)$$

$$|T(s)| = 1 \quad \Rightarrow \quad |G(s)| = 3$$

$$PM \cong 180° - 117° = 63°$$

But, we need at least 76° to eliminate any overshoot

Possible Solution: Lead Compensation

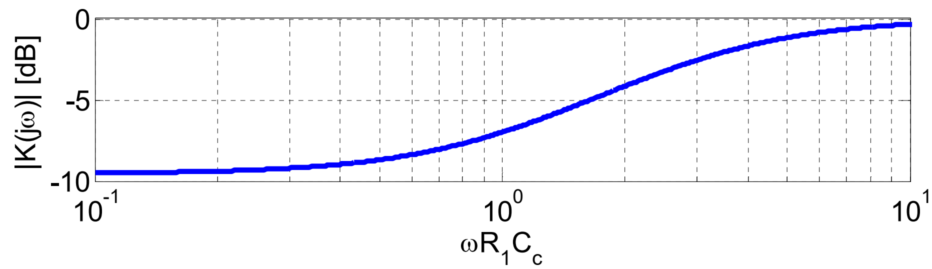


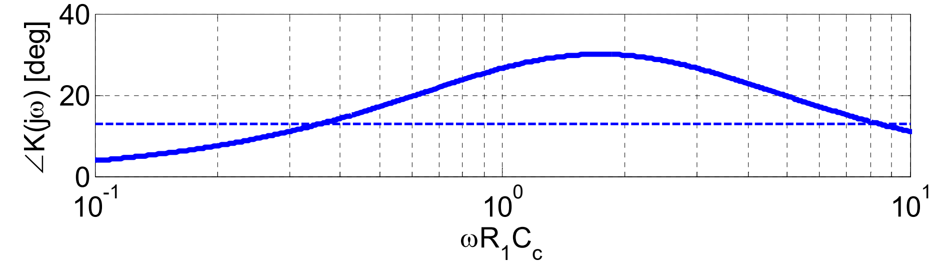
$$T(s) = \frac{R_2}{R_1 || \frac{1}{sC_c} + R_2} G(s) = K(s)G(s)$$

$$K(s) = \frac{R_2}{\frac{R_1}{1 + sR_1C_c} + R_2} = \frac{R_2}{R_1 + R_2} \cdot \frac{1 + sR_1C_c}{1 + s(R_1||R_2)C_c}$$

For $R_1 = 2R_2$: $\qquad z_1 = -\frac{1}{R_1C_c} \qquad p_1 = -\frac{3}{R_1C_c}$

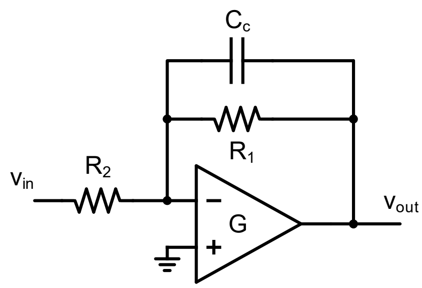
Bode Plot of K(s) for $R_1 = 2R_2$





- The feedback network gives us a phase lead that improves the PM
- If we size C_c such that $\omega_u \cong 0.25/R_1C_c$, we get the extra 13° we need

But, How About the Closed-Loop Gain?

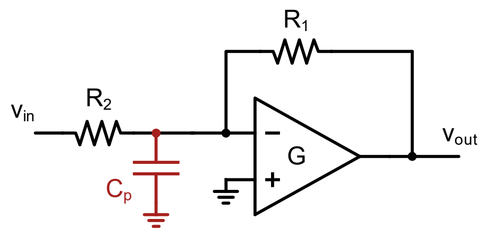


$$A_{CLI}(s) = -\frac{R_1 || \frac{1}{sC_c}}{R_2} = -\frac{R_1}{R_2}\frac{1}{1 + sR_1C_c}$$

In our example: $\omega_u \cong 0.25/R_1C_c$ $\qquad \frac{1}{R_1C_c} \cong 4\omega_u$

- Conclusion: No big deal, we get another closed-loop pole way past the original -3dB corner (which is about $1.28\omega_u$)
- We'll sacrifice a little bit of bandwidth, but we have our desired response

Another Example

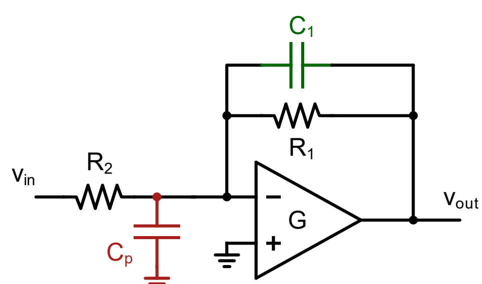


$$T(s) = \frac{R_2 || \frac{1}{sC_p}}{R_2 || \frac{1}{sC_c} + R_1} G(s) = K(s)G(s)$$

$$K(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{1 + s(R_1||R_2)C_p}$$

- Bad news: The extra pole in the loop may reduce the phase margin

Simple Remedy



$$T(s) = \frac{R_2 || \frac{1}{sC_p}}{R_2 || \frac{1}{sC_p} + R_1 || \frac{1}{sC_1}} G(s) = K(s)G(s)$$

$$K(s) = \frac{\frac{R_2}{1 + sR_2C_p}}{\frac{R_2}{1 + sR_2C_p} + \frac{R_1}{1 + sR_1C_1}} = \frac{R_2}{R_2 + R_1} \quad if \;\; R_1C_1 = R_2C_p$$

- If C_p is not exactly know, this requires some tweaking…

Summary

- Phase margin is the most widely used “proxy” for quantifying the stability margin of a feedback system
- First order system
  - Trivial; the phase margin is approximately 90º
- Second order system
  - There is a one-to-one mapping between phase margin and the Q of the closed-loop poles
  - A maximally flat response requires a phase margin of 65º
  - A critically damped response requires a phase margin of 76º
- Higher orders systems
  - Are typically approximated as second order systems
  - The extra high-frequency poles and zeros reduce the phase margin; this can be captured via an equivalent shift of the second pole to a lower frequency

Chapter 16

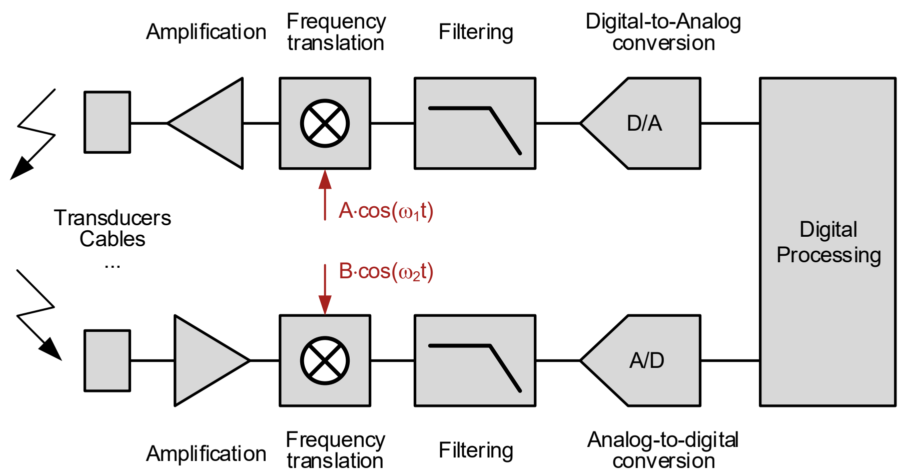
Oscillators

Boris Murmann

Stanford University

References:
Maloberti, Chapter 14, Section 14.3
Texas Instruments, Design of Op Amp Sine Wave Oscillators

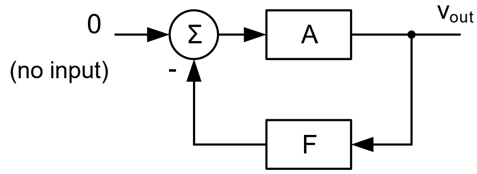
Motivation



- Most electronic systems require oscillators
  - Radios (above example), watches, microprocessor systems, etc.

How to Build an Oscillator?

- Key to all forms of oscillators is feedback
- The stability issues that bothered us in designing amplifiers are here being used to create steady-state oscillations



$T = AF$

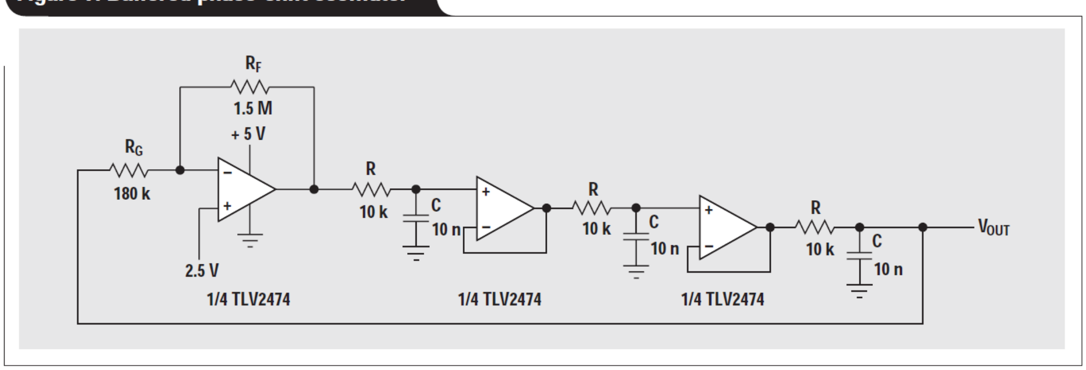
- Barkhausen criterion (1921):

A oscillator circuit will sustain steady-state oscillations at frequencies for which its gain around the loop is equal to unity in magnitude and the overall phase shift around the loop is 0° or an integer multiple of 360°.

→ T=AF must have 180° degrees of phase shift (plus integer multiple of 360°)

Phase Shift Oscillator

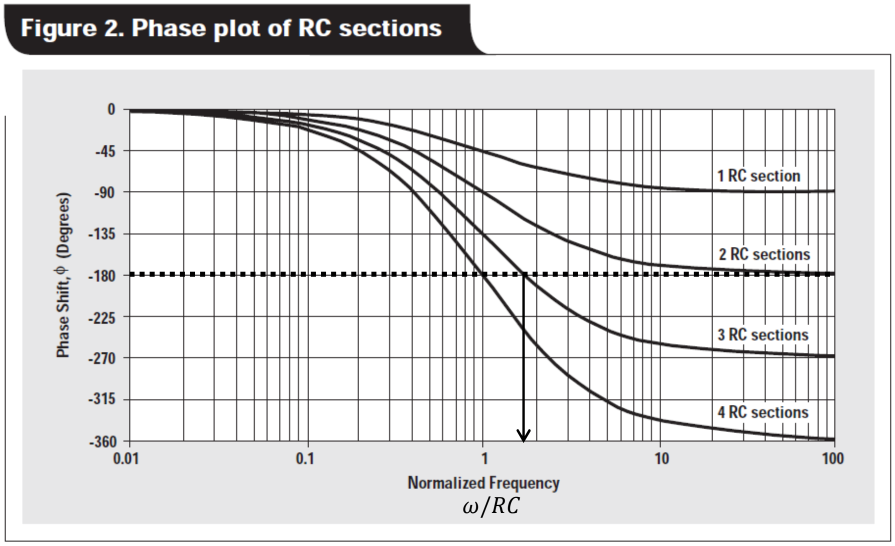
Figure 7. Buffered phase-shift oscillator



$$T(s) \cong \frac{R_F}{R_G} \frac{1}{(1+sRC)^3}$$

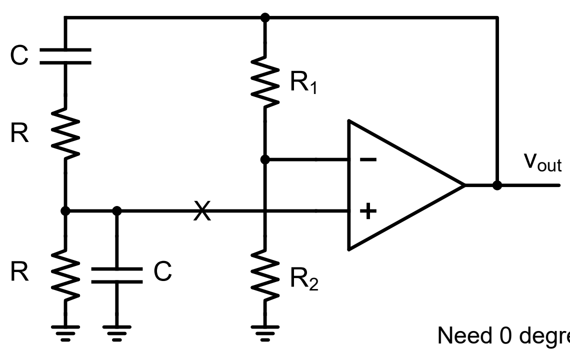
Need 180 degrees of phase shift from this term to enable oscillation

- As we already know, the poles land on the $j\omega$ axis for $R_F/RG = 8$
- The Barkhausen criterion is met at this point



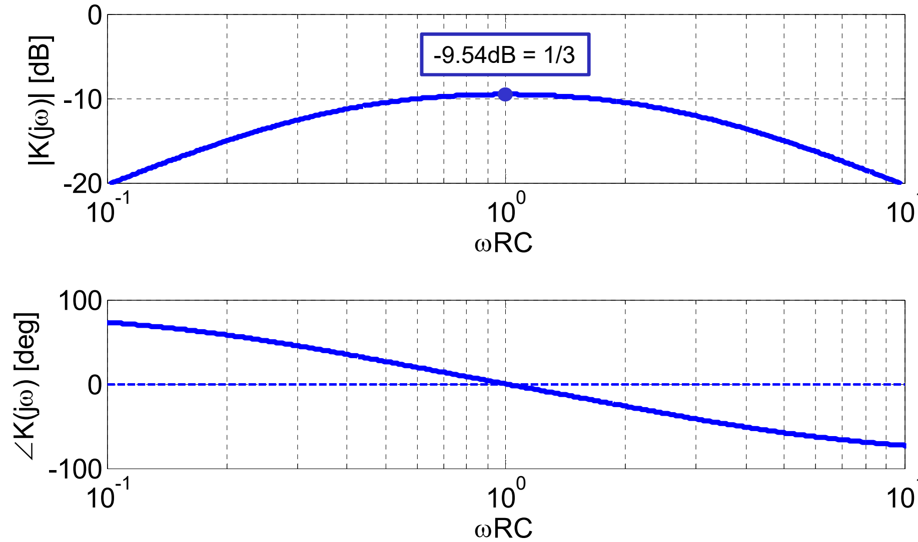
- The oscillation frequency is determined by the point where the total phase shift of the RC sections is -180°

Wien Bridge Oscillator



Need 0 degrees of phase shift from this term to enable oscillation

$$T(s) \cong -\frac{R_1+R_2}{R_2}\frac{sRC}{1+3sRC+s^2R^2C^2} = -\frac{R_1+R_2}{R_2}K(s)$$

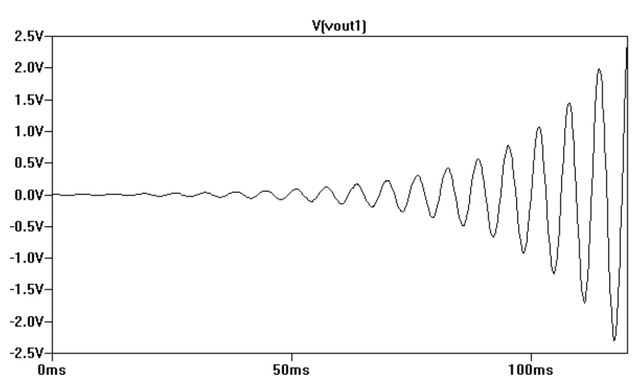


- The Barkhausen criterion is met when

$$\frac{R_1 + R_2}{R_2} = 3 \qquad R_1 = 2R_2$$

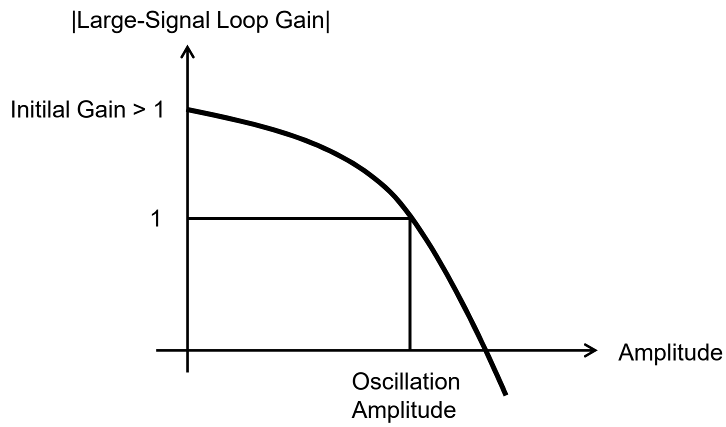
The Startup Problem

- Barkhausen is met during steady-state, i.e. when the circuit is oscillating
  - But how does it get into steady-state?
- For an oscillator to start up, it turns out that we need to push the closed loop poles into the RHP, to enable a growing envelope
  - The seed for this oscillation comes from any tiny "kick" applied to the circuit, e.g. turning on the power or thermal noise in the circuit

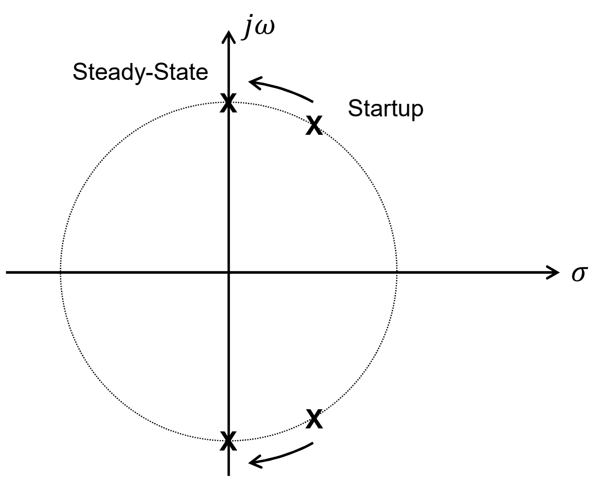


Amplitude Limiting

- The waveform grows until nonlinearities begin to reduce the loop gain
- The steady state amplitude is determined by the point where the large signal loop gain is unity, satisfying the Barkhausen criterion

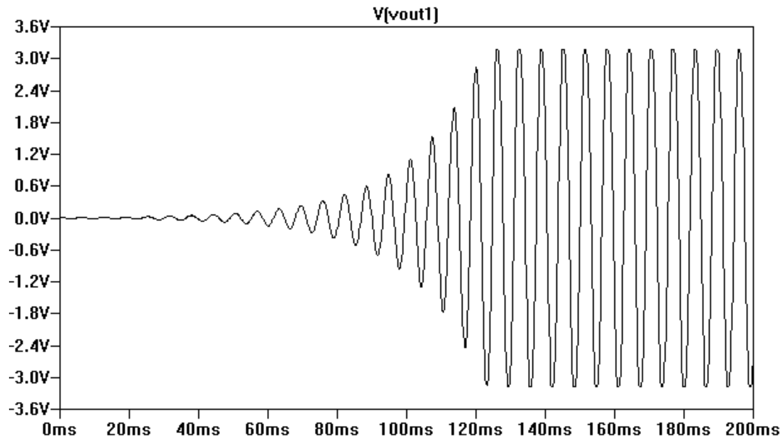


s-Domain Perspective

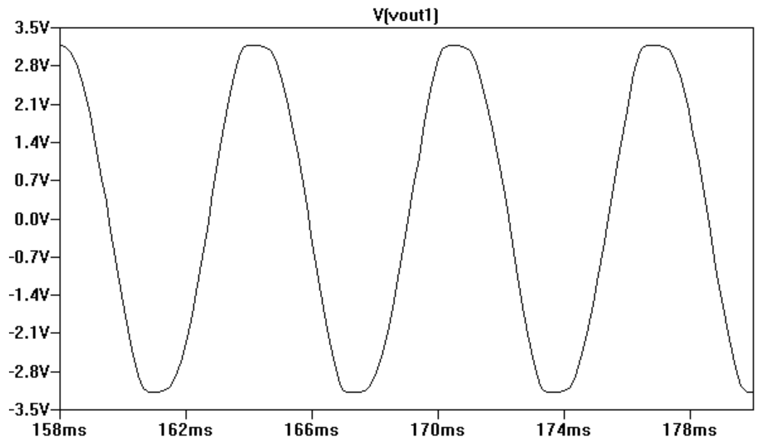


- This plot must be taken with a grain of salt, because we are dealing with a nonlinear system…

Startup with $R_1 = 2.1R_2$

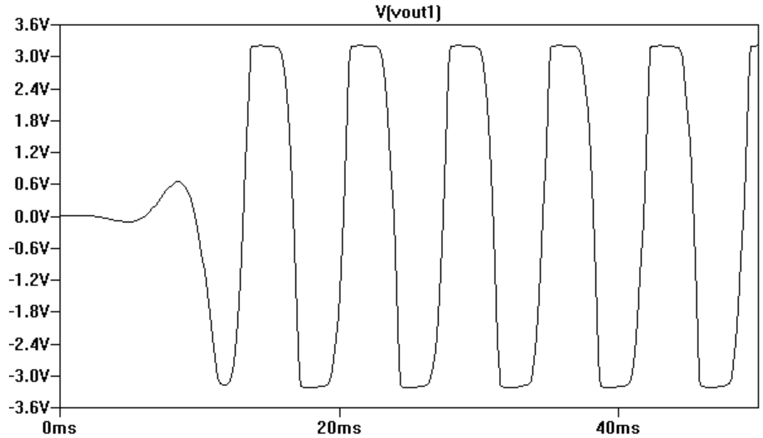


Steady-State Waveform



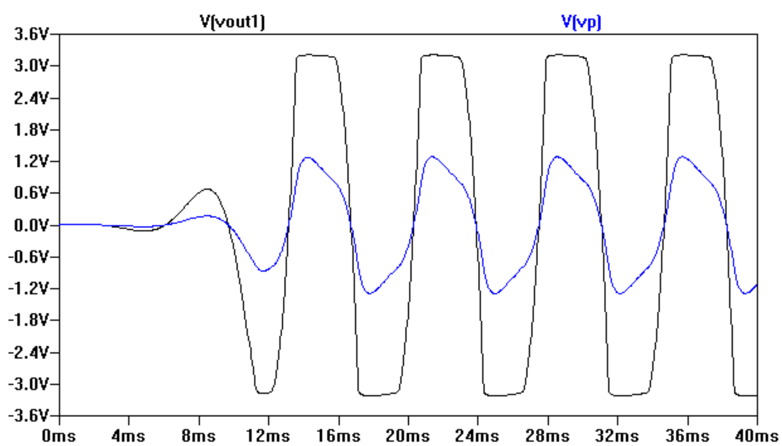
- Opamp is clipping (its supply voltage is +/-5V)

Startup with $R_1 = 3R_2$



- Startup is much faster (why?)
- Opamp clips hard; output looks more like a square wave

Startup with $R_1 = 3R_2$

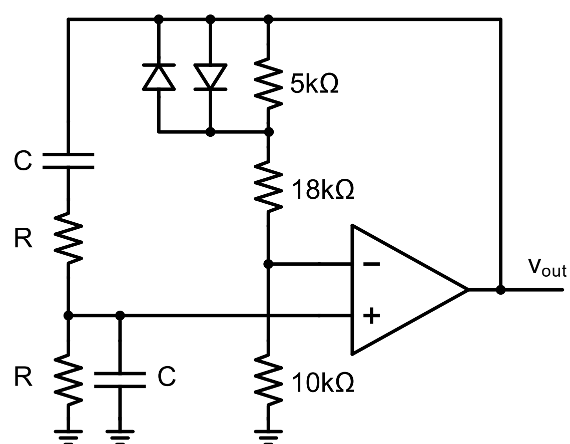


- The waveform at the positive input of the opamp looks somewhat nicer
  - Why?

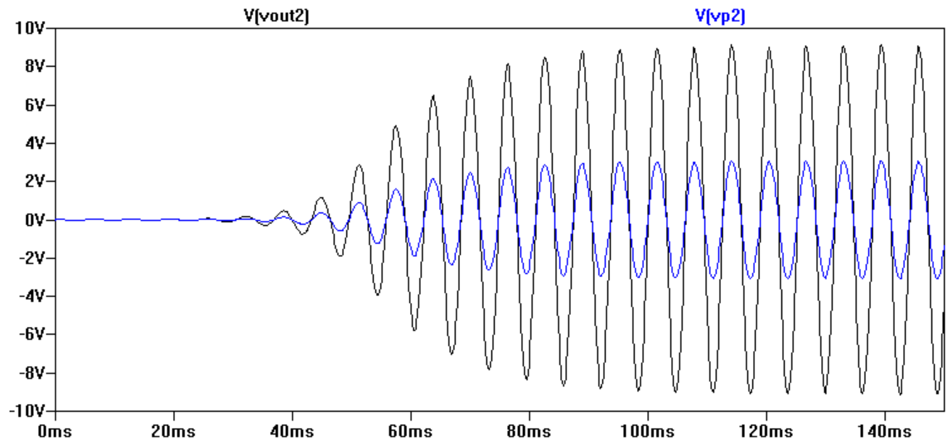
Need for Proper Amplitude Limiting

- We want the oscillator to start up reasonably fast and reliably
- We do not want the amplitude to be defined by the opamp's "random" clipping behavior, which may not be reproducible
- Practical Wien Bridge oscillators incorporate a well-defined mechanism for amplitude limiting
- Examples
  - Back-to-back diodes
  - Automatic gain control (AGC) loop
  - Adding a light bulb (!) to the feedback network

Amplitude Limiting with Diodes

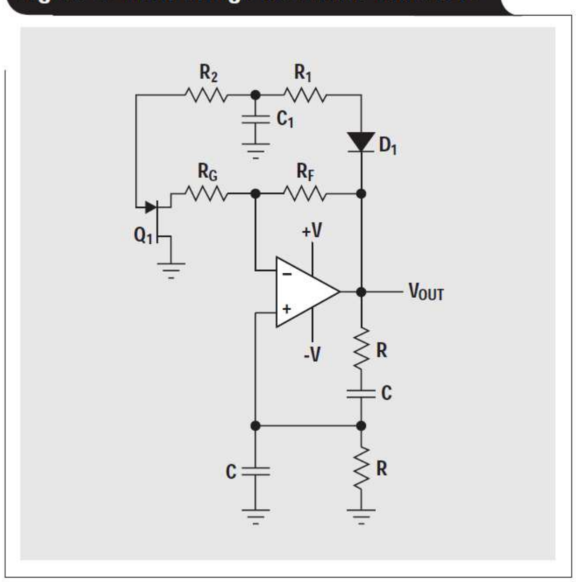


Startup with Diodes



(Opamp supplies increased to +/-15V; so that the opamp does not clip)

Figure 5. Wien-bridge oscillator with AGC

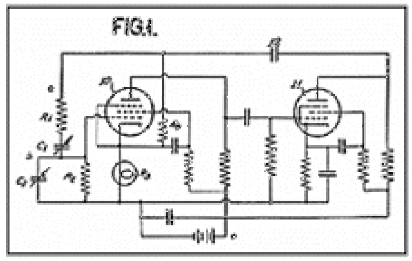


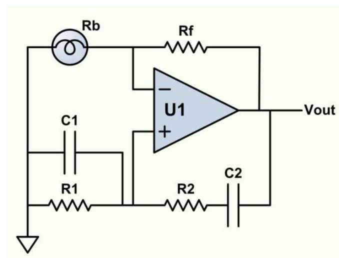
- Yields a lower distortion sinusoid than the diode-based circuit

HP200A

http://en.wikipedia.org/wiki/HP200A

- First HP product
- William Hewlett's MS thesis



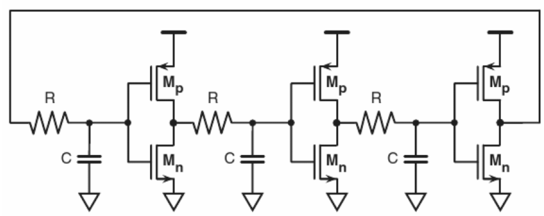


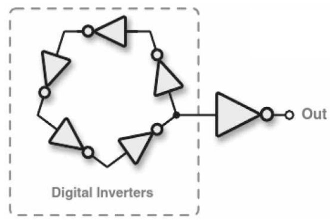
As the oscillation grows, R_b heats up until it becomes equal to $R_f/2$

More on Oscillators

- Ring Oscillator
- LC Oscillator
- Crystal Oscillator
- Relaxation Oscillator

Ring Oscillator

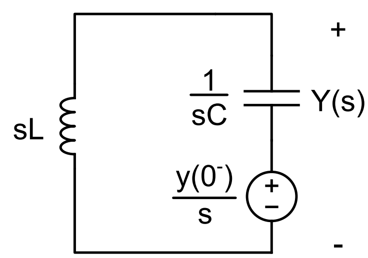




[Maloberti]

- In principle, not too different from a phase shift oscillator
- Use an odd number of stages (180° phase shift); remaining phase shift comes from RC delay
  - With an even number of stages, there is no inversion around the loop at DC and the circuit is simply a latch → more later
- Practical implementations often don't use explicit RC, but rely on the resistance and capacitance of the MOSFETs
  - Oscillation frequency is somewhat harder to predict
  - Can scale frequency down by using more inverters

Ideal Parallel LC Circuit ("LC Tank")



$$Y(s) = \frac{y(0^-)}{s}\frac{sL}{sL + \frac{1}{sC}} = y(0^-)\frac{s}{s^2 + \frac{1}{LC}} \qquad \mathcal{L}^{-1}\left\{\frac{s}{s^2 + \omega_0^2}\right\} = u(t)\cos(\omega_0 t)$$

$$y(t) = y(0^-)u(t)\cos(\omega_0 t) \qquad \omega_0 = \frac{1}{\sqrt{LC}}$$

- A non-zero initial condition will suffice to create an everlasting oscillation

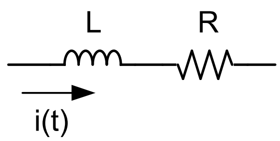
Quality Factor of Inductors and Capacitors

- Unfortunately real inductors and capacitors dissipate energy
- The "quality factor" for these components is defined as

$$Q = 2\pi \frac{Peak\ energy\ stored}{Energy\ dissipated\ per\ cycle} = \frac{E_{max}}{E_{diss}}$$

- For an inductor, the losses are well-modeled using a series resistor

$$Z = R + j\omega L$$

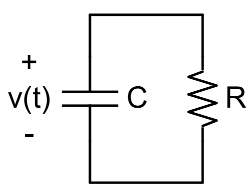


$$E_{max} = \frac{1}{2} L i_{max}^2$$

$$E_{diss} = P_{diss} T = \frac{1}{2} i_{max}^2 R \cdot \frac{2\pi}{\omega}$$

$$\boxed{Q_L = \frac{\omega L}{R} = \frac{Im(Z)}{Re(Z)}}$$

- For a capacitor, the losses are typically modeled using a parallel resistor



$$E_{max} = \frac{1}{2} C v_{max}^2$$

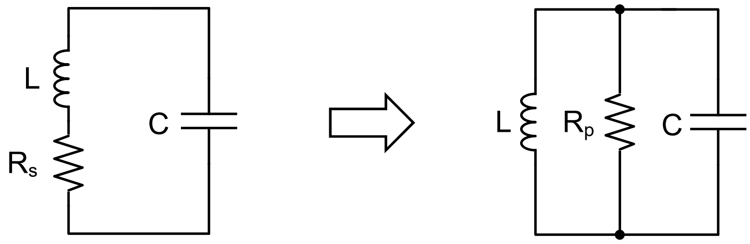
$$E_{diss} = P_{diss} T = \frac{\frac{1}{2} v_{max}^2}{R} \cdot \frac{2\pi}{\omega}$$

$$Y = \frac{1}{R} + j\omega C$$

$$\boxed{Q_C = \omega C R = \frac{Im(Y)}{Re(Y)}}$$

- In practice, inductor losses tend to be much more significant than capacitor losses, so we will only consider the former in our analysis

LC Tank with Inductor Losses



- Working with a series resistance can be annoying in a parallel circuit
- It is therefore common to approximate the losses with a parallel resistor

$$Z_s = R_s + j\omega L$$

$$Q_s = \frac{\omega L}{R_s}$$

$$Z_p = \frac{j\omega L R_p}{R_p + j\omega L} = \frac{j\omega L R_p}{R_p + j\omega L}\frac{\left(R_p - j\omega L\right)}{\left(R_p - j\omega L\right)}$$
$$= \frac{\omega^2 L^2 R_p}{R_p^2 + \omega^2 L^2} + j\frac{\omega L R_p^2}{R_p^2 + \omega^2 L^2}$$

$$Q_p = \frac{R_p}{\omega L}$$

$$Z_s = R_s + j\omega L$$

$$Z_p = \frac{R_p}{\frac{R_p^2}{\omega^2 L^2} + 1} + j\frac{\omega L \frac{R_p^2}{\omega^2 L^2}}{\frac{R_p^2}{\omega^2 L^2} + 1}$$

$$Z_p = \frac{R_p}{Q_p^2 + 1} + j\frac{\omega L Q_p^2}{Q_p^2 + 1}$$

- Assuming $Q_p >> 1$, the imaginary parts are approximately equal and

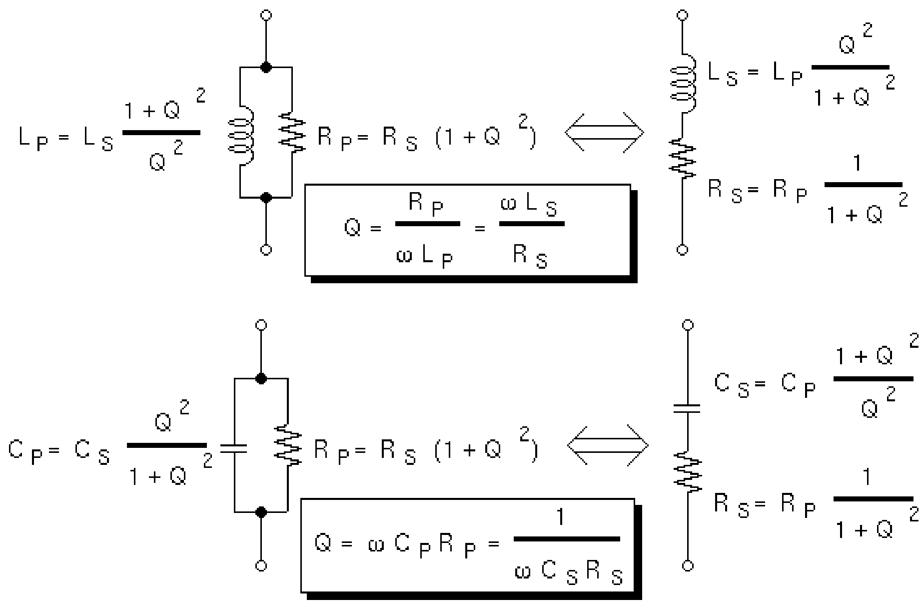
$$\boxed{R_p \cong R_s Q_p^2}$$

- Also note that

$$Q_p = \frac{R_p}{\omega L} \cong \frac{R_s Q_p^2}{\omega L} = \frac{Q_p^2}{Q_s} \Rightarrow Q_p \cong Q_s$$

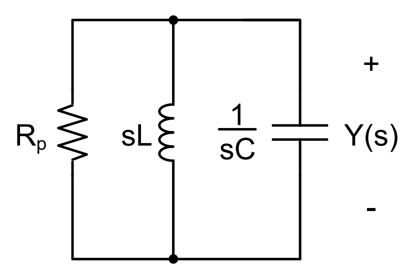
- Finally, note that since the quality factor is frequency dependent, the above approximation holds only at one single frequency
  - This is OK for analyzing narrow-band circuits, like oscillators

Summary on Parallel to Series Conversion



http://wcalc.sourceforge.net/cgi-bin/parallel_rl.cgi
http://wcalc.sourceforge.net/cgi-bin/parallel_rc.cgi

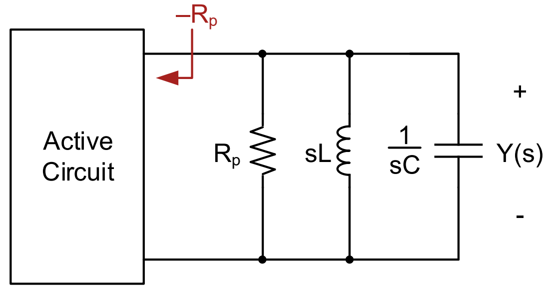
Back to Our Circuit



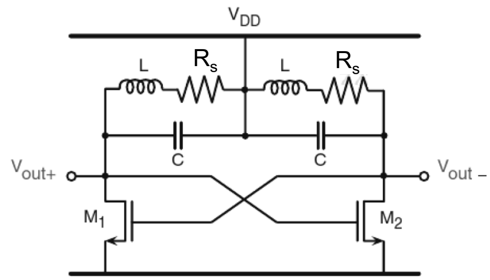
- Analyzing this circuit with some initial condition (as we did before) yields a decaying sinusoid

$$\mathcal{L}^{-1}\left\{\frac{s+a}{(s+a)^2+\omega_0^2}\right\} = u(t)\mathrm{e}^{-\mathrm{at}}\cos(\omega_0 t)$$

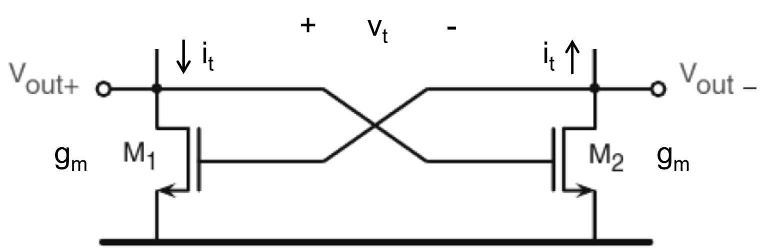
Eliminating R_p



- Basic implementation:



[Maloberti]



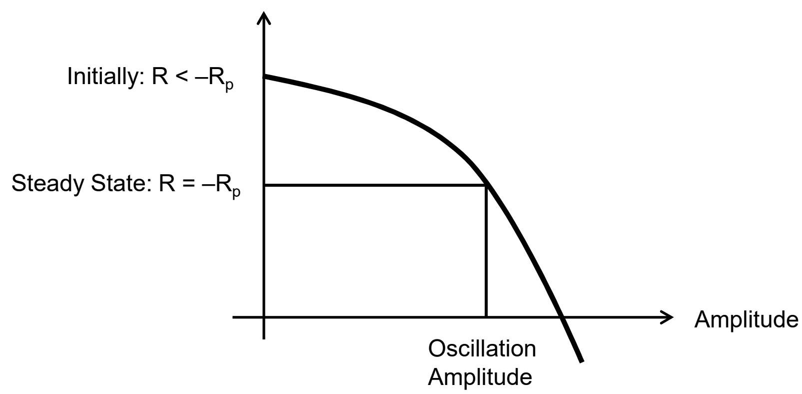
$$v_t = v_{gs2} - v_{gs1}$$

$$i_t = g_m v_{gs1} \qquad -i_t = g_m v_{gs2} \qquad \Rightarrow v_{gs2} = -v_{gs1}$$

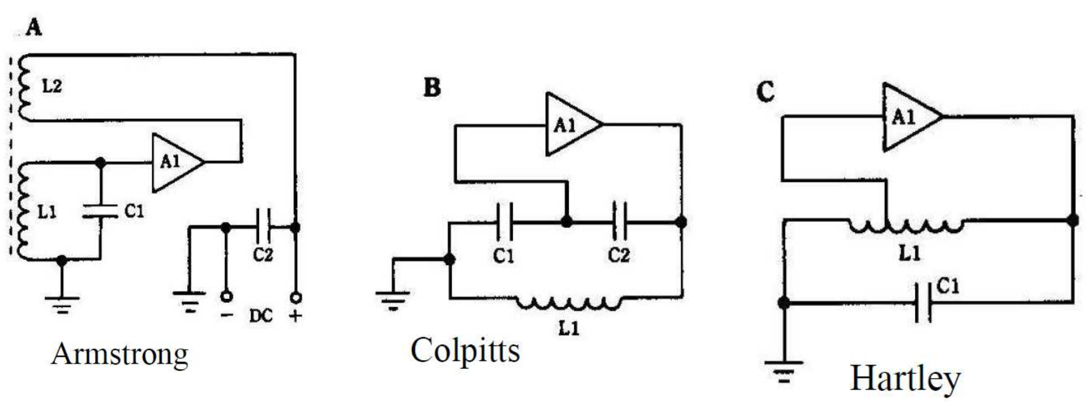
$$R = \frac{v_t}{i_t} = -\frac{1}{g_m} - \frac{1}{g_m} = -\frac{2}{g_m}$$

Amplitude Limiting

- For proper startup, the net resistance must be negative initially
- As the amplitude grows, the negative resistance shrinks in magnitude and becomes equal to $-R_p$ in steady-state



Other Architectures (Many More Exist)



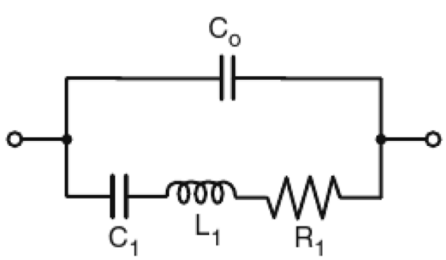
(Biasing details omitted)

- These architectures can be analyzed using feedback theory or using a negative resistance approach
- The two analysis methods are complementary; sometimes one is more convenient/intuitive than the other

Quartz Crystals

- Quartz shows piezoelectric behavior: Applying a voltage induces a deformation (a fraction of μm) and vice versa
- A properly cut crystal has a mechanical resonance with a very precisely defined frequency and low drift (a few ppm/°C)
- Main application is in wristwatches, clocking for digital integrated circuits, and frequency generation for radio transmitters and receivers

Electrical Equivalent

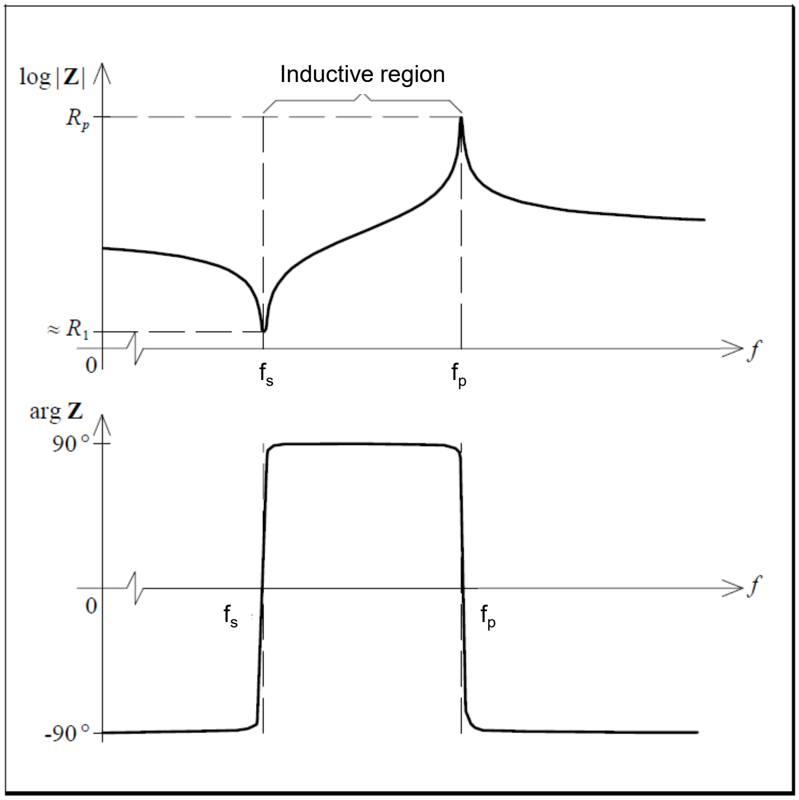


Typical values:

$$C_o = 3pF$$
$$L_1 = 0.25H$$
$$C_1 = 40fF$$
$$R_1 = 50\Omega$$

- Key: The quality factor of the series RLC network is extremely high, on the order of 10^4 to 10^6
- The circuit exhibits a "series resonance" and a "parallel resonance," which are very close to one another (within a small fraction of a percent)

$$Z(s) = \frac{s^2 + s\frac{R_1}{L_1} + \omega_s^2}{sC_o\left(s^2 + s\frac{R_1}{L_1} + \omega_p^2\right)} \qquad \omega_s = \frac{1}{\sqrt{L_1C_1}} \qquad \omega_p = \sqrt{\frac{C_1 + C_0}{L_1C_oC_1}} \cong \omega_s\left(1 + \frac{C_1}{C_0}\right)$$



Example: Operation at the Series Resonance

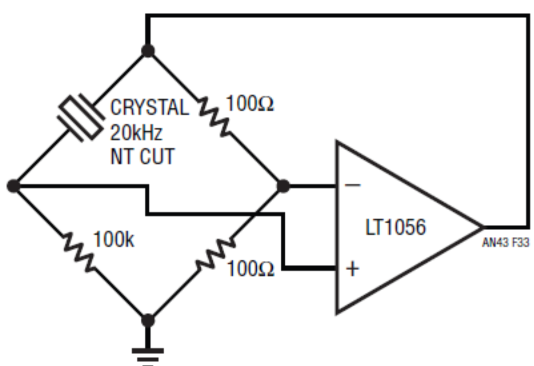


Figure 33. Bridge-Based Crystal Oscillator

http://cds.linear.com/docs/en/application-note/an43f.pdf

Example: Pierce Oscillator

- Operates the crystal in its inductive region
- Main advantage of this configuration is its simplicity, robustness, and the ability to “pull” the frequency slightly (via C_1 and $C_2 \rightarrow C_o$)
- R_f (large resistor) serves to bias the inverter in its linear region

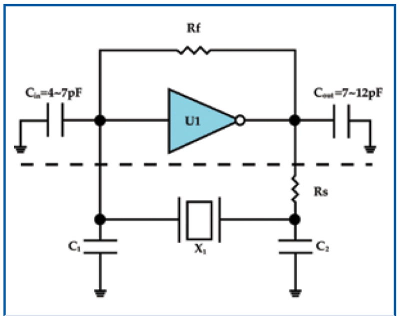
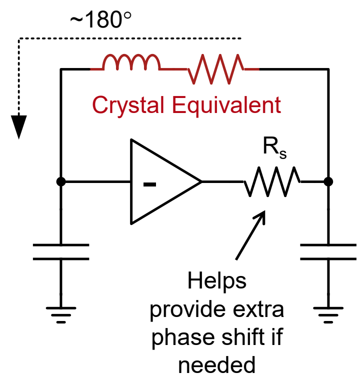
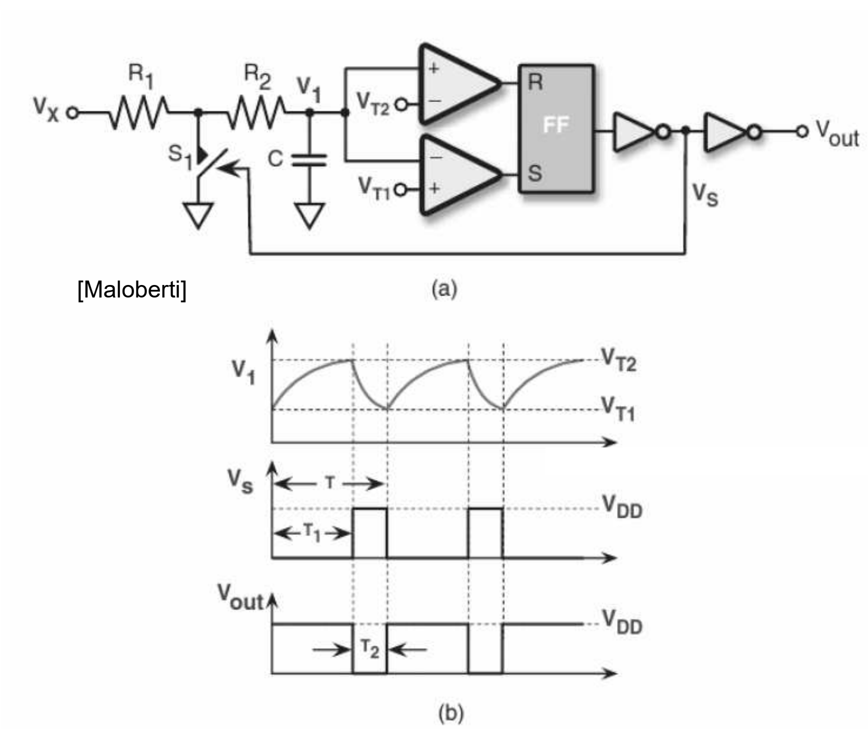


Figure 3: Pierce-Gate Showing Internal Input and Output Capacitances

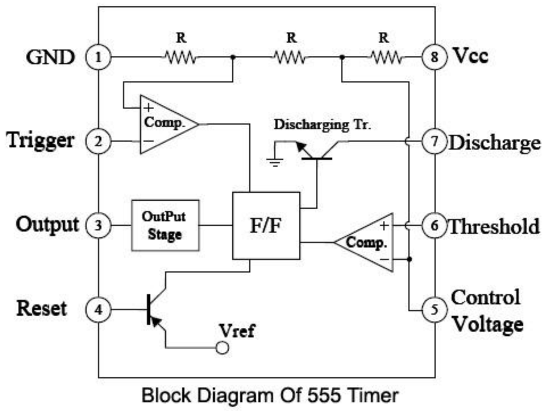


http://www.crystek.com/documents/appnotes/Pierce-GateIntroduction.pdf

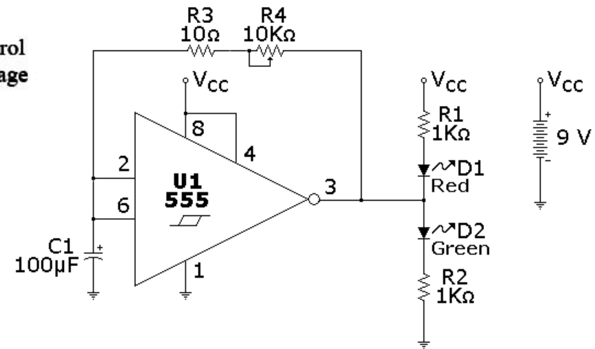
Relaxation Oscillator



555 Timer



Block Diagram Of 555 Timer



http://www.allaboutcircuits.com/vol_6/chpt_8/3.html

Chapter 17

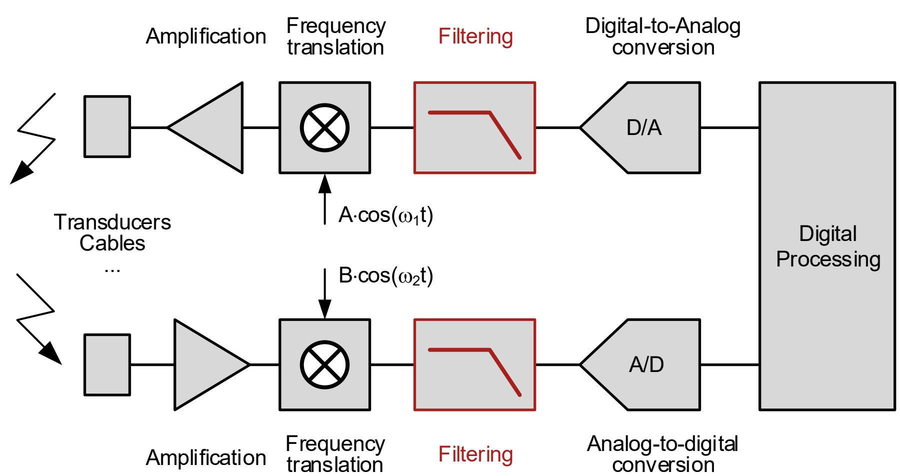
Filters

Boris Murmann

Stanford University

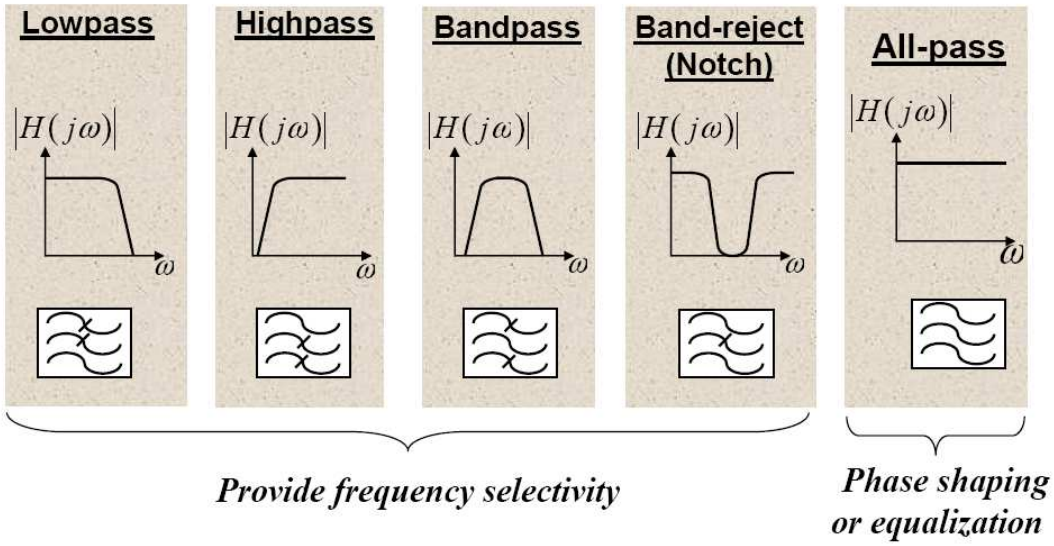
Reference: Analog Devices, Linear Circuit Design Handbook, Chapter 8
Texas Instruments, Op Amps for Everyone

Motivation



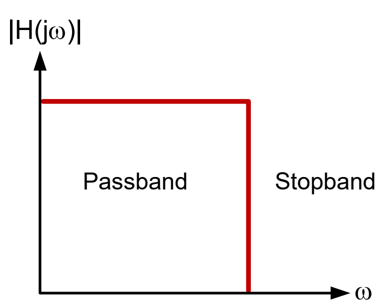
- Filters are used in many systems, for a variety of purposes
  - Frequency band selection in radios, removal of noise or unwanted interference (e.g. 60Hz notch filter), smoothing of signals, …

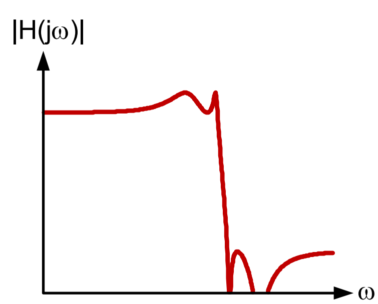
Filter Types



The Filter Approximation Problem

- Ideal Filter
  - Brick-wall characteristic
  - Flat magnitude response in the passband
  - Infinite attenuation in the stopband
- Practical filter
  - Ripple in either or both the passband and stopband
  - Limited attenuation in the stopband

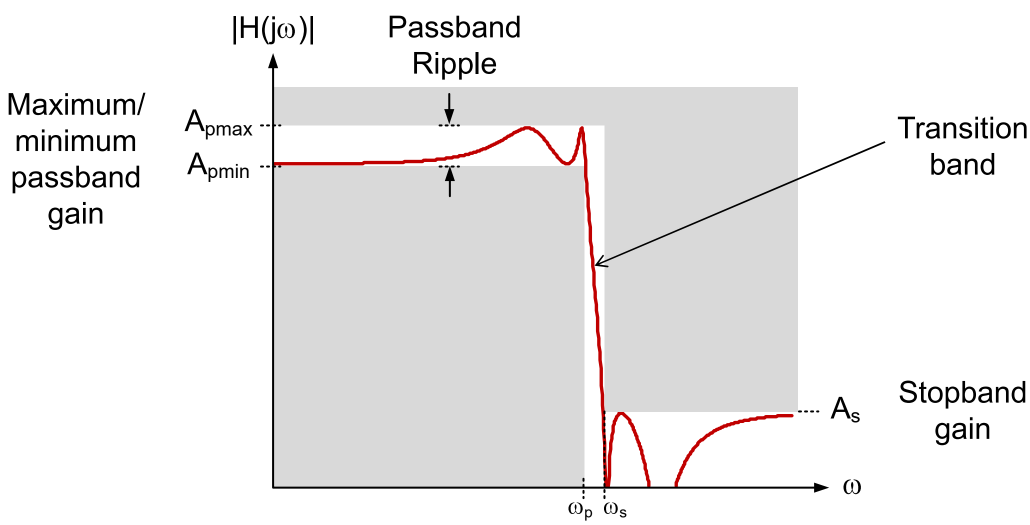




Filter Design

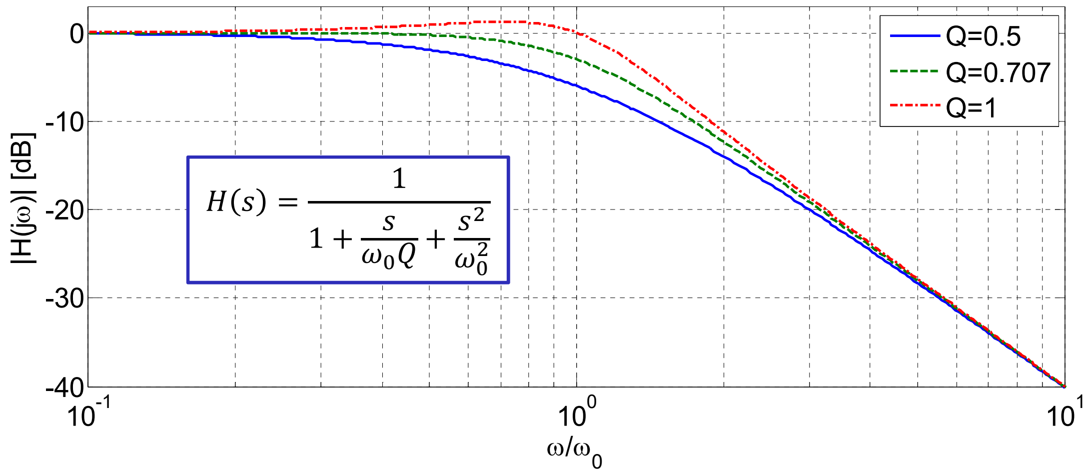
- Ideal filters are non-causal or otherwise impractical
- No global optimization techniques known
- In practice, chose from several known solutions
  - Butterworth, Elliptic, Bessel, …
- The overall goal of filter design is to approximate the ideal response by one that implements a reasonable compromise between filter complexity (number of poles and zeros) and approximation error
- Filter design, in general, requires a compromise between magnitude response, phase response, step response, complexity, etc.
- It is common to base a filter design on a lowpass prototype
  - Then “transform” into highpass or bandpass (more later)

Lowpass Filter Template



- Specifications are fully defined by A_{pmin}, A_{pmax}, A_s, ω_p, ω_s

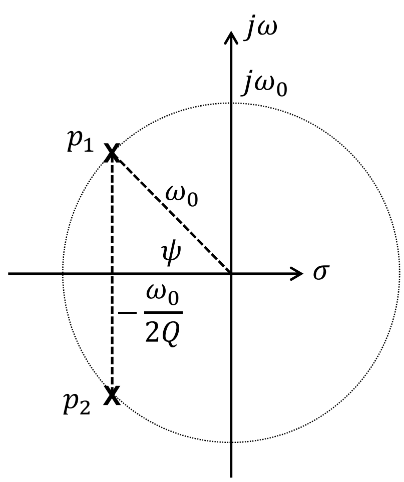
Re-Cap: Second Order Lowpass Response



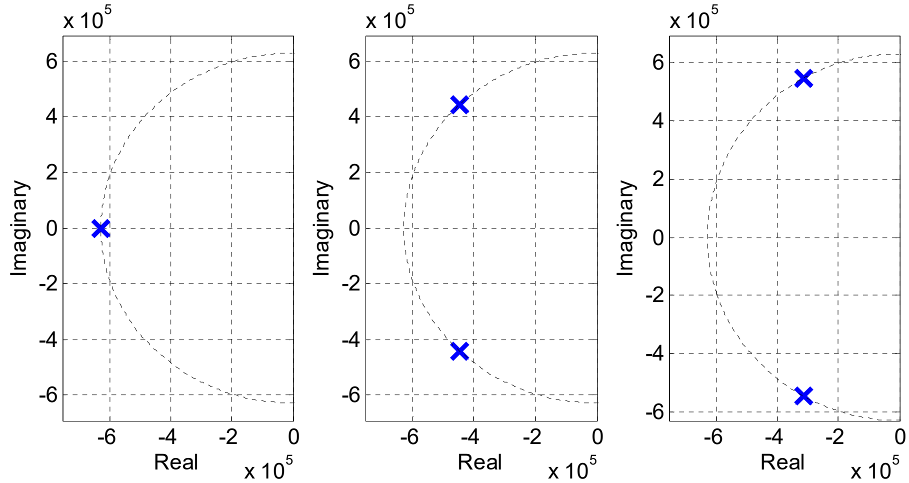
$$H(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

- Magnitude response is "maximally flat" (no peaking) for $Q = \frac{1}{\sqrt{2}}$

Pole Locations for $Q > 0.5$



$$\psi = acos\left(\frac{\frac{\omega_0}{2Q}}{\omega_0}\right) = acos\left(\frac{1}{2Q}\right)$$



$$Q = 0.5$$
$$\psi = 0°$$

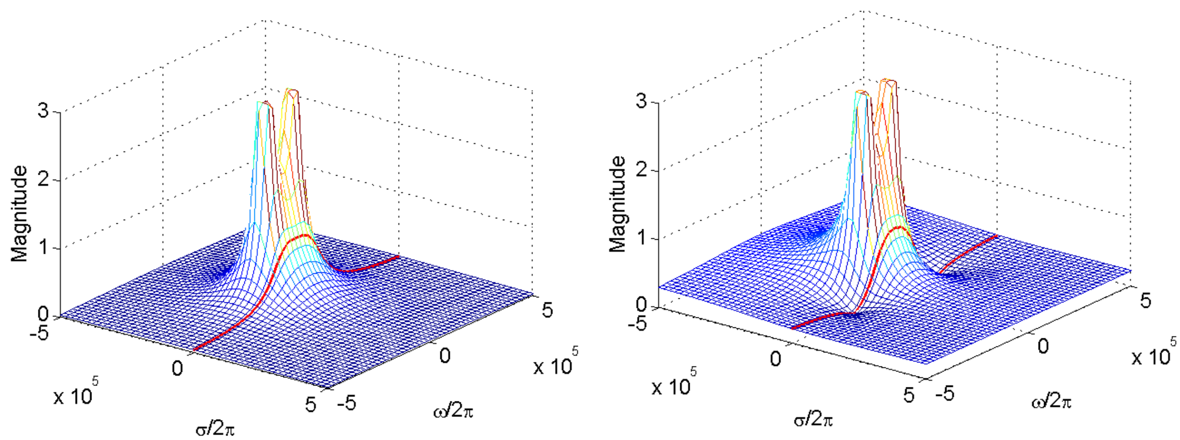
$$Q = \frac{1}{\sqrt{2}}$$
$$\psi = 45°$$

$$Q = 1$$
$$\psi = 60°$$

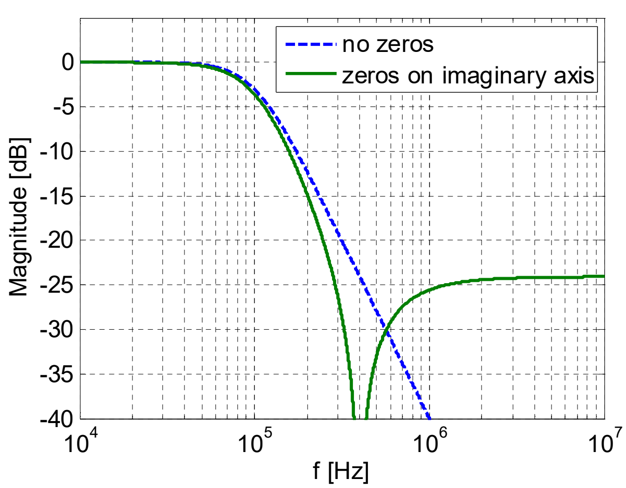
Improvements

- A maximally flat response is great, but how can we make the roll-off steeper?
- Let's look at
  - Imaginary zeros
  - Increasing the filter order
  - High-Q poles
  - High-Q poles and imaginary zeros

Adding Zeros on the Imaginary Axis



Bode Plot

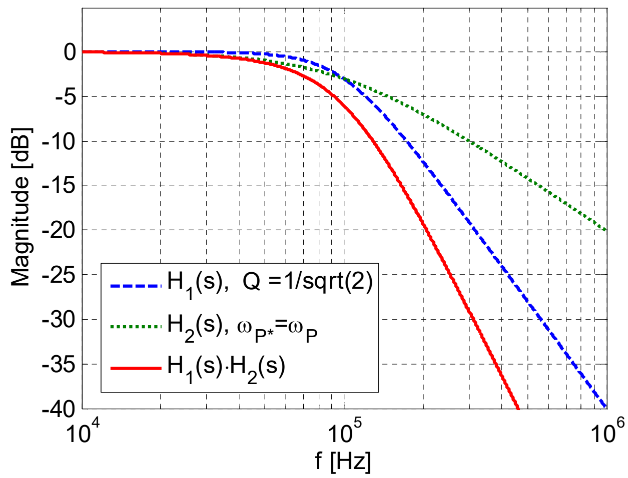


$$H(s)=\frac{1+\left(\frac{s}{\omega_Z}\right)^2}{1+\frac{s}{\omega_P Q}+\left(\frac{s}{\omega_P}\right)^2}$$

$$\left|H(j\omega)\right|_{\omega\to\infty}=\left(\frac{\omega_P}{\omega_Z}\right)^2$$

- Steeper roll-off at the expense of reduced stopband rejection

Adding Another Real Pole



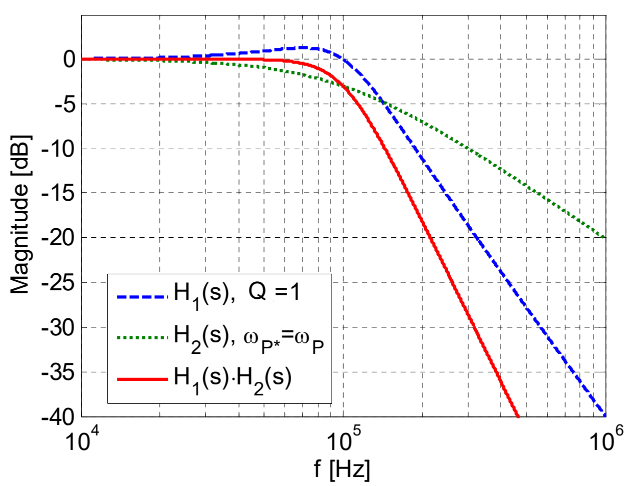
$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_P Q} + \left(\frac{s}{\omega_P}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \left(\frac{s}{\omega_{P^*}}\right)}$$

- As expected, steeper roll-off, but transition is not all that sharp
- Can fix this issue by increasing the Q of $H_1(s)$!

Utilizing Peaking in $H_1(s)$



$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_P Q} + \left(\frac{s}{\omega_P}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \left(\frac{s}{\omega_{P^*}}\right)}$$

- Win-win improvement
  - Passband flat, roll-off steeper

n^{th} Order Generalization

- Stephen Butterworth showed in 1930 that the magnitude response of an n^{th} order maximally flat lowpass filter is given by

$$|H(j\omega)| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_P}\right)^{2n}}}$$

- This magnitude response is monotonically decreasing and satisfies

$$\left.\frac{d^k |H(j\omega)|}{d\omega^k}\right|_{\omega=0} = 0 \quad \text{for} \quad 1 \le k \le 2n-1$$

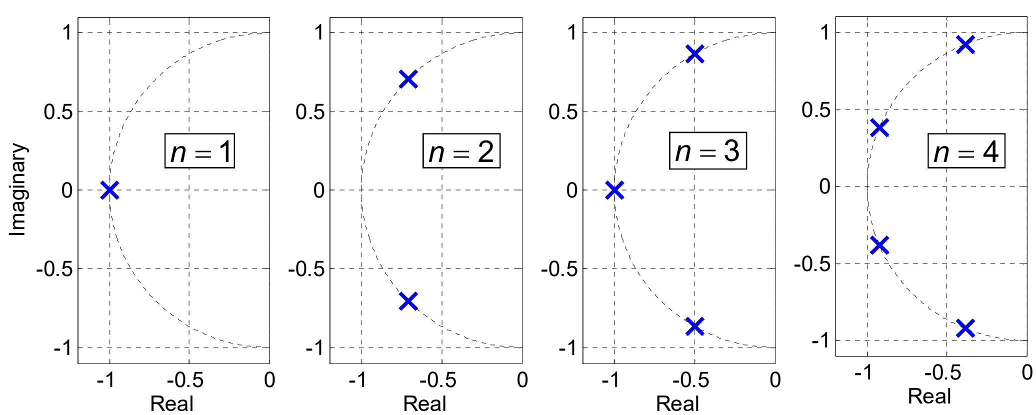
- The corresponding pole locations can be determined using

$$|H(s)|^2 = H(s)\cdot H(-s) = \frac{1}{1+\left(\frac{-s^2}{\omega_P^2}\right)^n} \qquad \frac{-s^2}{\omega_P^2} = (-1)^{1/n} = e^{\frac{j(2k-1)\pi}{n}} \qquad k = 1,2,3...,n$$

Pole Locations

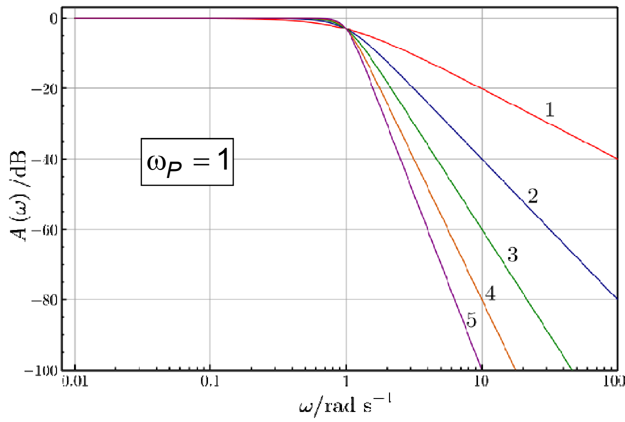
- The poles lie equally spaced (in angle) on a circle in the s-plane centered at the origin with radius ω_P
- The LHP roots are taken to be the poles of H(s), while those in the RHP are regarded as the poles of H(–s)

$\omega_P = 1$



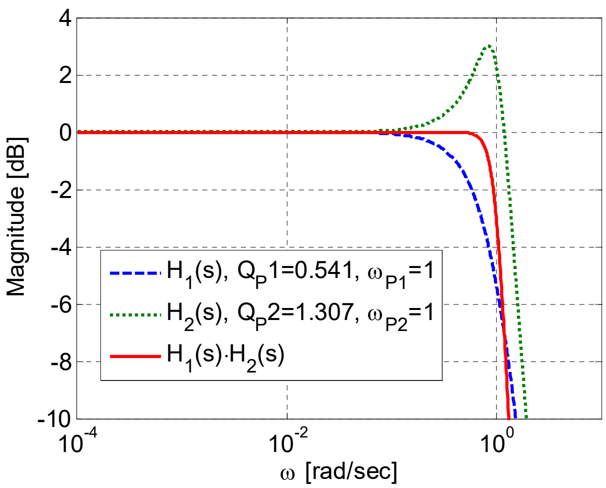
Magnitude Response and Coefficients

http://en.wikipedia.org/wiki/Butterworth_filter



n	Denominator Polynomial
1	$(s + 1)$
2	$s^2 + 1.4142s + 1$
3	$(s + 1)(s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)(s^2 + 1.8478s + 1)$
5	$(s + 1)(s^2 + 0.6180s + 1)(s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + 1.4142s + 1)(s^2 + 1.9319s + 1)$
7	$(s + 1)(s^2 + 0.4450s + 1)(s^2 + 1.2470s + 1)(s^2 + 1.8019s + 1)$
8	$(s^2 + 0.3902s + 1)(s^2 + 1.1111s + 1)(s^2 + 1.6629s + 1)(s^2 + 1.9616s + 1)$

A Closer Look at n=4



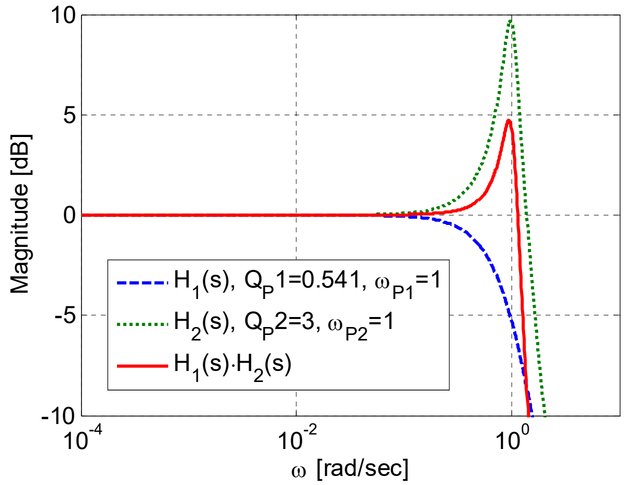
$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_{P1} Q_{P1}} + \left(\frac{s}{\omega_{P1}}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \frac{s}{\omega_{P2} Q_{P2}} + \left(\frac{s}{\omega_{P2}}\right)^2}$$

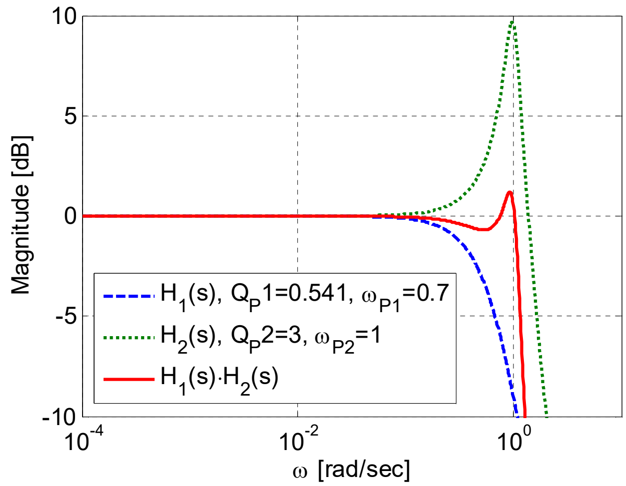
$$\psi = \cos^{-1}\left(\frac{1}{2Q_P}\right) \qquad Q_{P1} = \frac{1}{2\cos\left(22.5^\circ\right)} = 0.541 \qquad Q_{P2} = \frac{1}{2\cos\left(67.5^\circ\right)} = 1.307$$

Increasing Q_{P2}



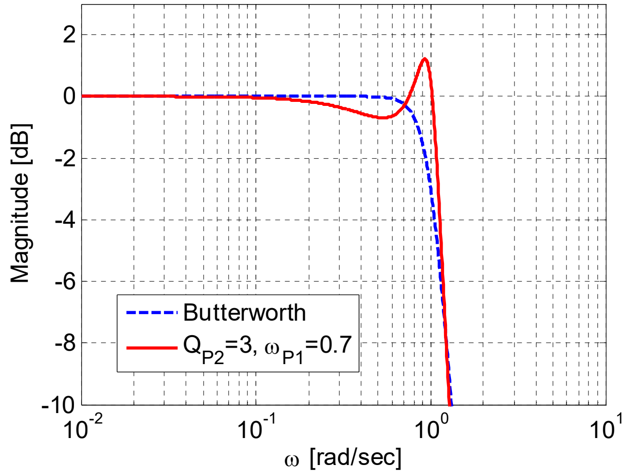
- Helps make the roll-off steeper, but introduces peaking
- We can try to alleviate this problem this by reducing ω_{P1}

Increased Q_{P2}, Reduced ω_{P1}



- This may not a bad choice of we can tolerate some peaking or ripple

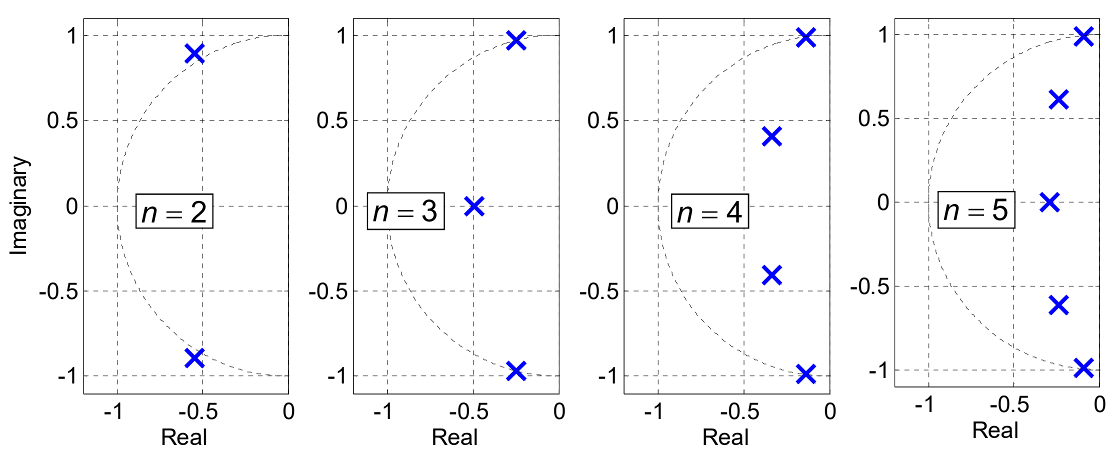
Comparison with Original Butterworth



- How can we optimize this situation, i.e. minimize the transition band for a given tolerable peaking (or "ripple") in the passband?

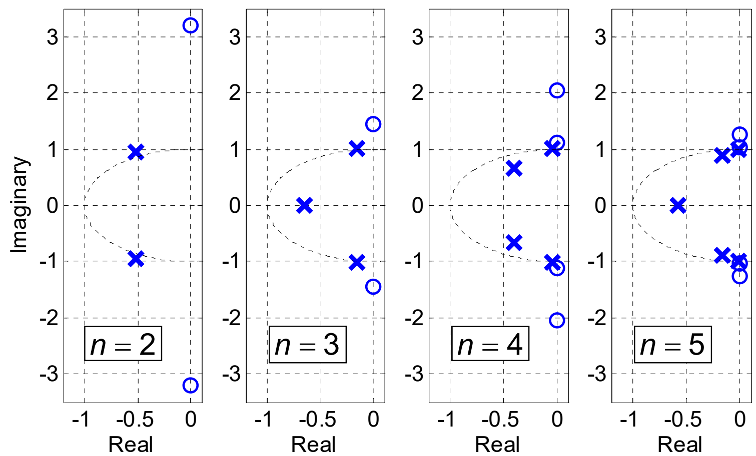
Chebyshev1 Filter Approximation

- Fortunately someone has already figure this out!
- The "Chebyshev1" filter approximation minimizes the error between the idealized response and the actual filter, with the passband ripple as a parameter (1dB for examples below)



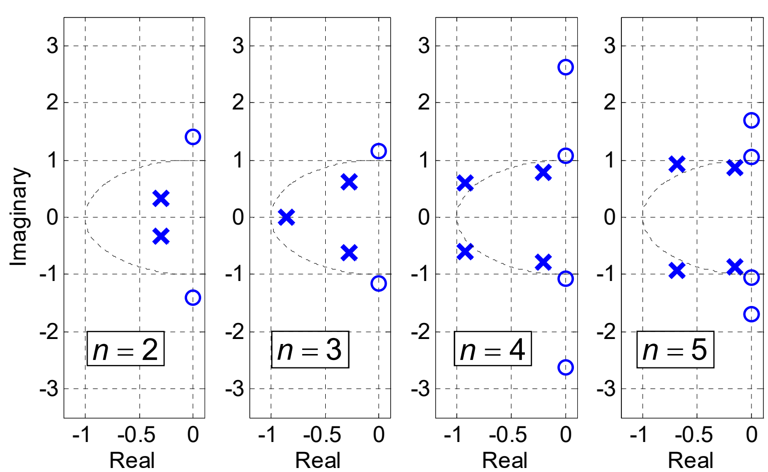
Elliptic (Cauer) Filter Approximation

- The Elliptic filter approximation combines our previous ideas and adds imaginary zeros to sharpen the transition band
- This approximation has the passband ripple and stopband attenuation as a parameter (1dB and 20dB, respectively, for example below)



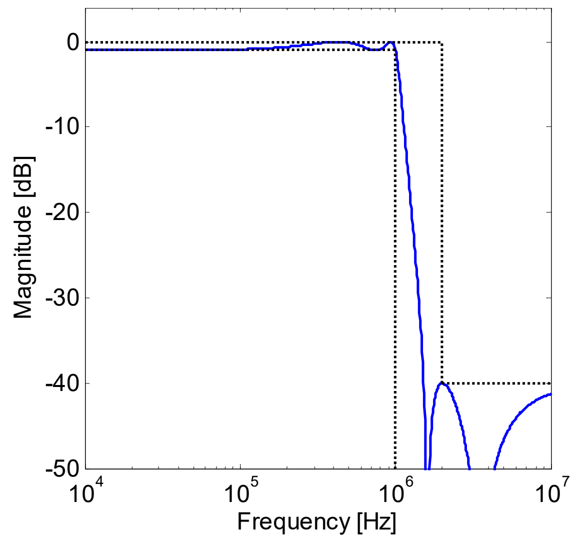
Chebyshev2 Filter Approximation

- No ripple in the passband, but finite stopband attenuation and ripple due to imaginary zeros
- This approximation takes the stopband attenuation as a parameter (20 dB in the example below)

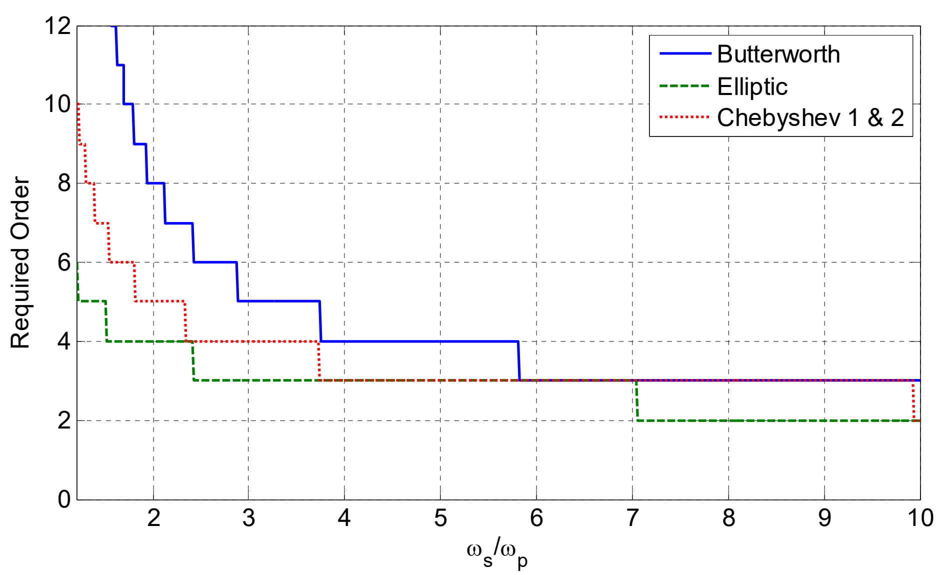


Matlab Design Example

```
wp=2*pi*1e6; % Passband edge
ws=2*pi*2e6; % Stopband edge
Rp=1;  % Passband ripple
Rs=40; % Stopband attenuation

% Determine required order and synthesize
[N, wp] = ellipord(wp, ws, Rp, Rs, 's');
[z, p, k] = ellip(N, Rp, Rs, wp, 's');

sys = zpk(z, p, k);
f = logspace(4, 7, 1000);
[mag, phase] = bode(sys, 2*pi*f);
db = 20*log10(reshape(mag, 1, length(f)));
figure(1)
semilogx(f, db, 'linewidth', 2);
```



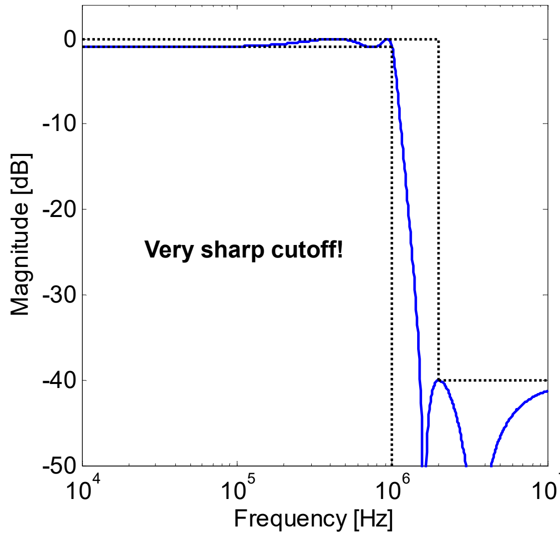
Filter Order for R_p=1dB, R_s=40dB



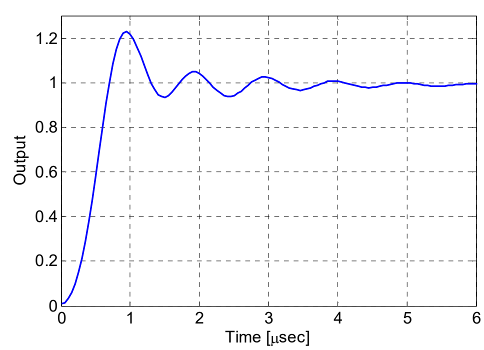
- Why not always use an Elliptic filter?
  - It is certainly the best choice if we consider the magnitude response only
  - But, there may be constraints on the step response; more later…

Matlab Design Example – Elliptic Filter

```
wp=2*pi*1e6; % Passband edge
ws=2*pi*2e6; % Stopband edge
Rp=1;  % Passband ripple
Rs=40; % Stopband attenuation

% Determine required order and synthesize
[N, wp] = ellipord(wp, ws, Rp, Rs, 's');
[z, p, k] = ellip(N, Rp, Rs, wp, 's');

sys = zpk(z, p, k);
f = logspace(4, 7, 1000);
[mag, phase] = bode(sys, 2*pi*f);
db = 20*log10(reshape(mag, 1, length(f)));
figure(1)
semilogx(f, db, 'linewidth', 2);
```

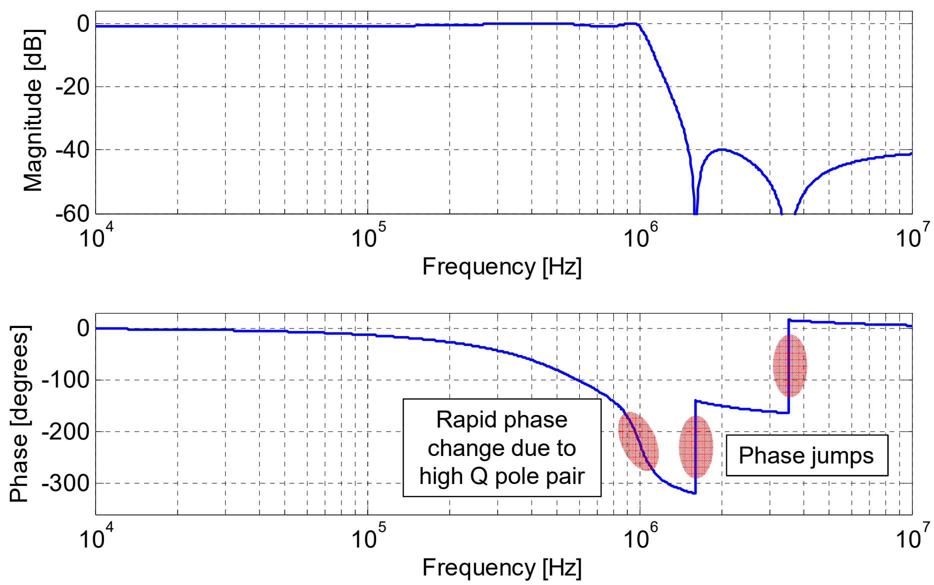


Step Response of Design Example



- Overshoot and other forms of pulse deformation can be problematic
  - Consider e.g. oscilloscopes, pulse-based data links, etc.
- The pulse deformation is mostly due to the fact that different frequency components pass the filter with different time delays
  - This is called phase distortion
- Let's first have a look at the phase response of our filter

Phase Response of Design Example



Phase Jumps due to Imaginary Zeros

$$\underbrace{\left(1-\frac{s}{+j\omega_z}\right)\left(1-\frac{s}{-j\omega_z}\right)}_{\text{Complex conjugate pair on the imaginary axis}}=\left(1+\frac{s^2}{\omega_z^2}\right)=\left(1+\frac{(j\omega)^2}{\omega_z^2}\right)=\left(1-\frac{\omega^2}{\omega_z^2}\right)$$

$$\measuredangle\left(1-\frac{\omega^2}{\omega_z^2}\right)=\begin{cases}0^\circ & \omega\le\omega_z\\ 180^\circ & \omega>\omega_z\end{cases}$$

- As seen on the previous slide, the phase jumps occur at the frequencies of the zeros

Phase Distortion (1)

- Consider a filter with transfer function

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)}$$

- Apply two sine waves at different frequencies

$$v_{in}(t) = A_1 \sin(\omega_1 t) + A_2 \sin(\omega_2 t)$$

$$v_{out}(t) = A_1 |H(j\omega_1)| \sin(\omega_1 t + \phi(\omega_1)) + A_2 |H(j\omega_2)| \sin(\omega_2 t + \phi(\omega_2))$$

$$= A_1 |H(j\omega_1)| \sin\left(\omega_1 \left[t + \underbrace{\frac{\phi(\omega_1)}{\omega_1}}_{\text{Phase delay } t_{d1}}\right]\right) + A_2 |H(j\omega_2)| \sin\left(\omega_2 \left[t + \underbrace{\frac{\phi(\omega_2)}{\omega_2}}_{\text{Phase delay } t_{d2}}\right]\right)$$

Phase Distortion (2)

- Assuming that the difference between $|H(j\omega_1)|$ and $|H(j\omega_2)|$ is small, the "shape" of the time-domain output signal will be preserved as long as

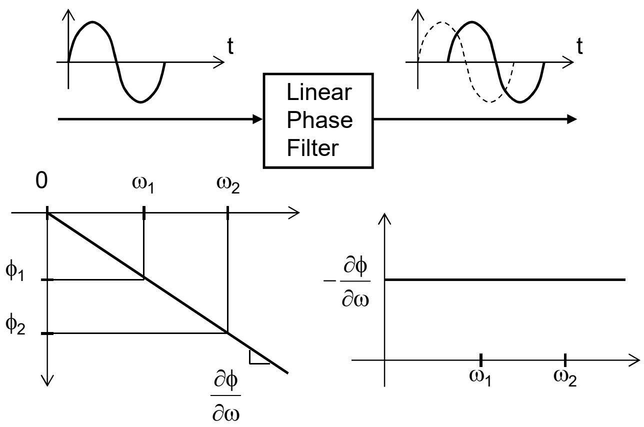
$$\frac{\phi(\omega_1)}{\omega_1} - \frac{\phi(\omega_2)}{\omega_2} = 0$$

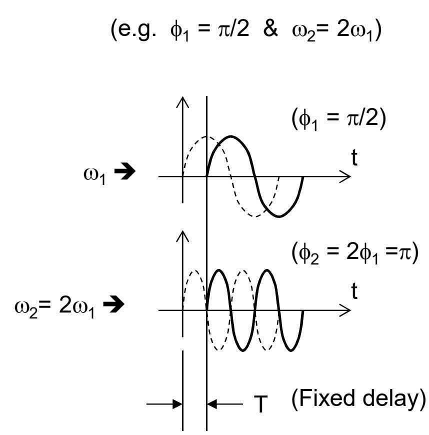
- This condition is satisfied for

$$\phi(\omega) = T \cdot \omega \qquad T = \text{constant}$$

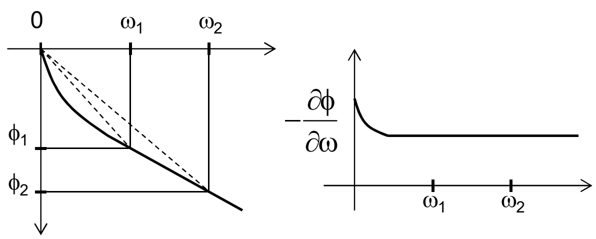
- A filter with this characteristic is called "linear phase"

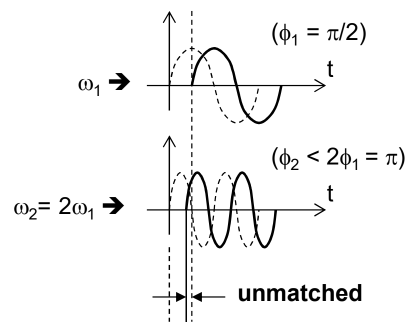
Delay with Linear Phase





Delay with Nonlinear Phase





$$\frac{\phi(\omega_1)}{\omega_1} \neq \frac{\phi(\omega_2)}{\omega_2}$$

- Phase distortion occurs whenever the phase is nonlinear, i.e. the derivative of the phase is not constant
- The (negative) derivative of the phase is also called "group delay" or τ_g
- Note that for a linear phase filter, we have $\tau_g = \tau_d = \text{const.}$

Bessel Filter Approximation

- Optimized for maximally flat group delay
- Poles only, no zeros
- Poles are relatively low Q
- Poor magnitude roll-off

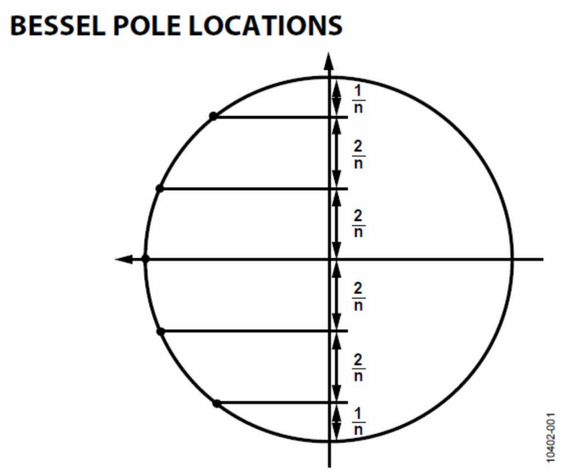
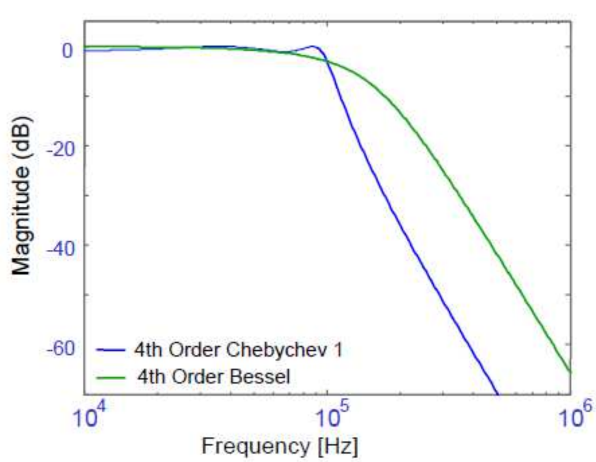


Figure 1. Bessel Pole Locations

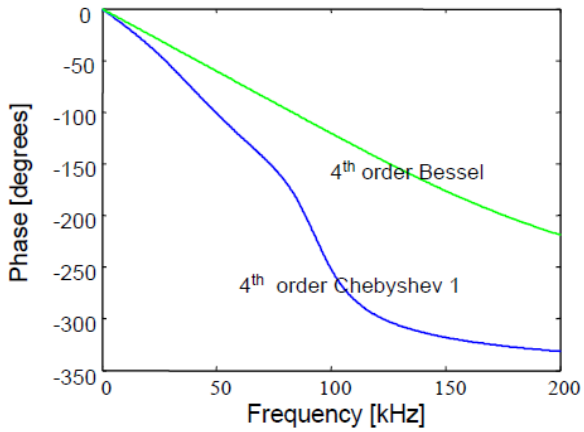
n = number of poles

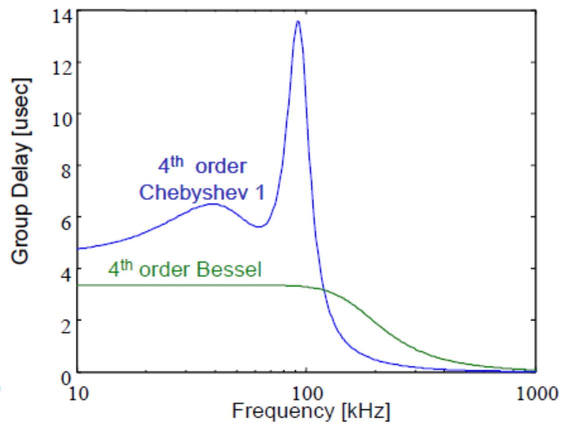
Comparison: Bessel vs. Chebyshev1



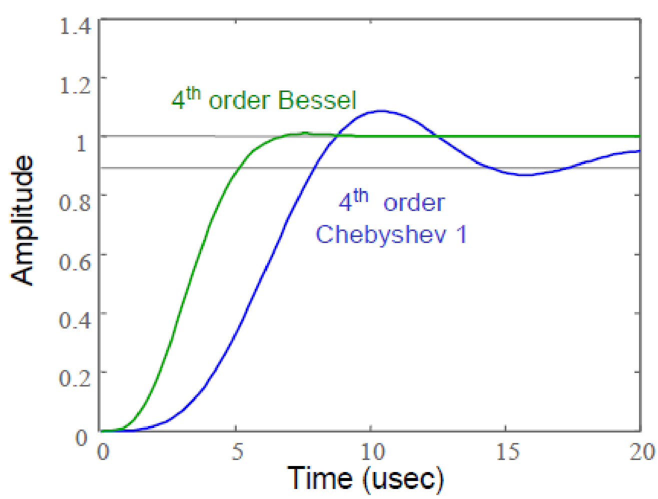
- Lowpass filters with 100 kHz passband
- Both filters are 4th order with the same -3 dB frequency
- Passband ripple of 1dB for Chebyshev I

Phase and Group Delay



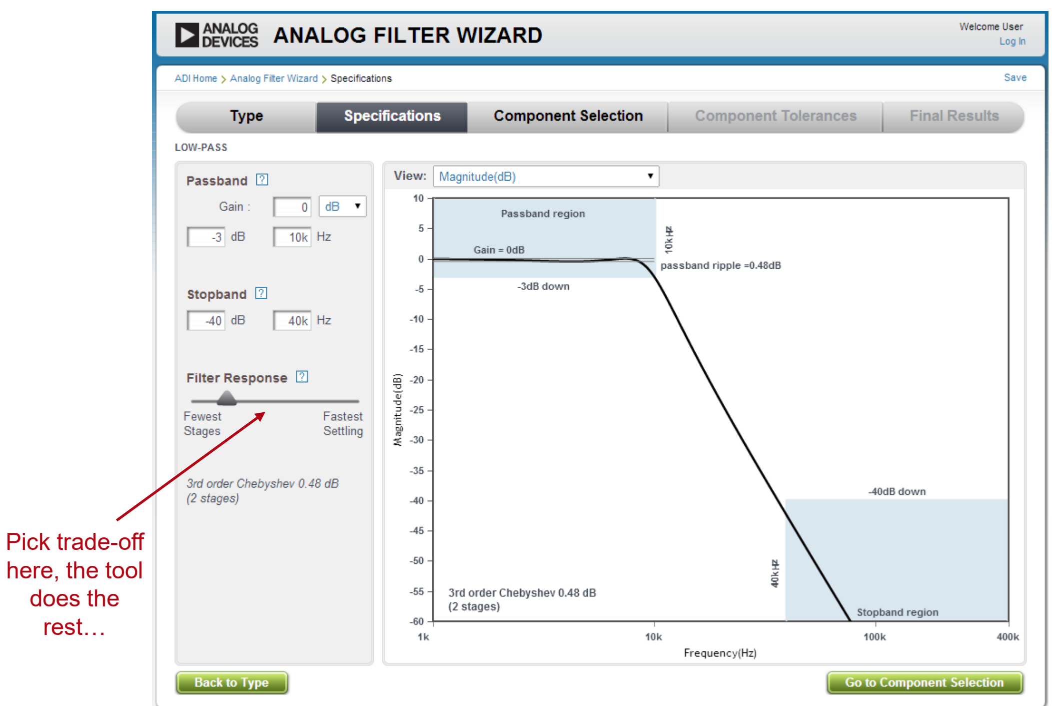


Step Response



Summary

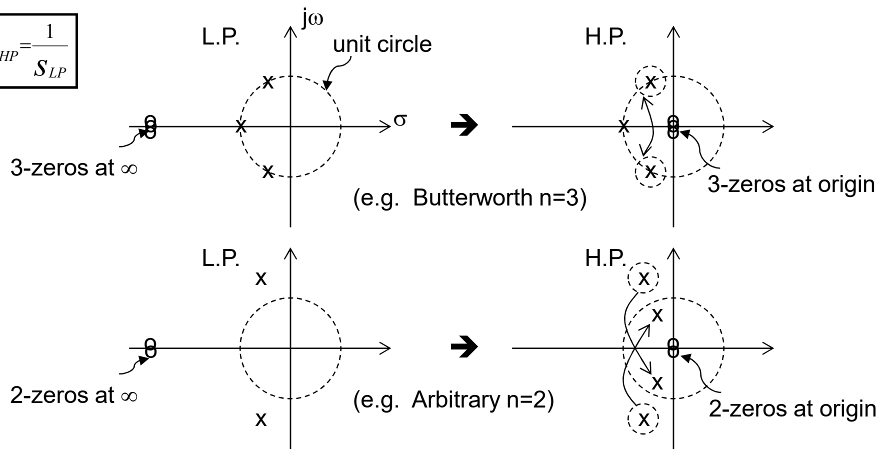
- We can either get a sharp roll-off in the frequency domain or a well-behaved step response
  - Not both at the same time
- Elliptic filters offer the steepest magnitude roll-off, but have the worst step response
- Bessel filters have a maximally flat group decay and hence the best step response; but they suffer from a very poor magnitude roll-off
- A Butterworth filter lies somewhere in-between; i.e. reasonable compromise between roll-off and ringing in the step response



http://www.analog.com/designtools/en/filterwizard/#/specifications

Lowpass to Highpass Transformation

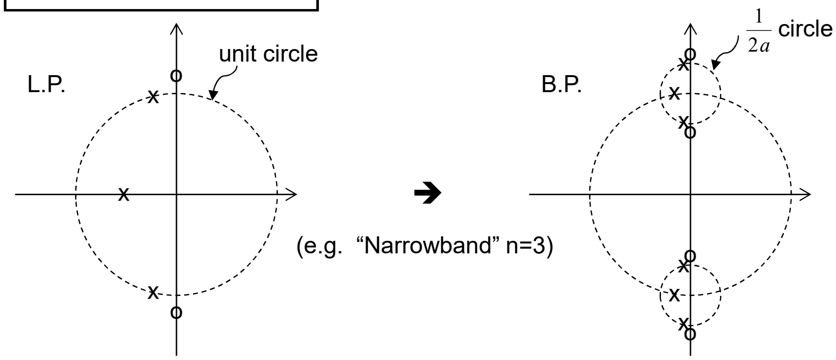
$$\boxed{S_{HP} = \frac{1}{S_{LP}}}$$



The s-domain poles and zeros simply become inverted. As shown by the examples, zeros at infinity move to the origin, and finite-valued poles become $|1/\text{pole}_{LP}|$ in magnitude and become conjugates (flips between quadrant II & III). The mapping boundary is the normalized unit circle (ω_0 of the response).

Lowpass to Bandpass Transformation

$$\boxed{S_{BP} = \frac{S_{LP}}{2a} \pm j\sqrt{1-\left(\frac{S_{LP}}{2a}\right)^2} \approx \frac{S_{LP}}{2a} \pm j}$$ where $$\boxed{a = \frac{f_m}{\Delta f} = \text{“Q”}\ ;\ f_m = \sqrt{f_1 f_2}\ ;\ \Delta f = f_2 - f_1}$$

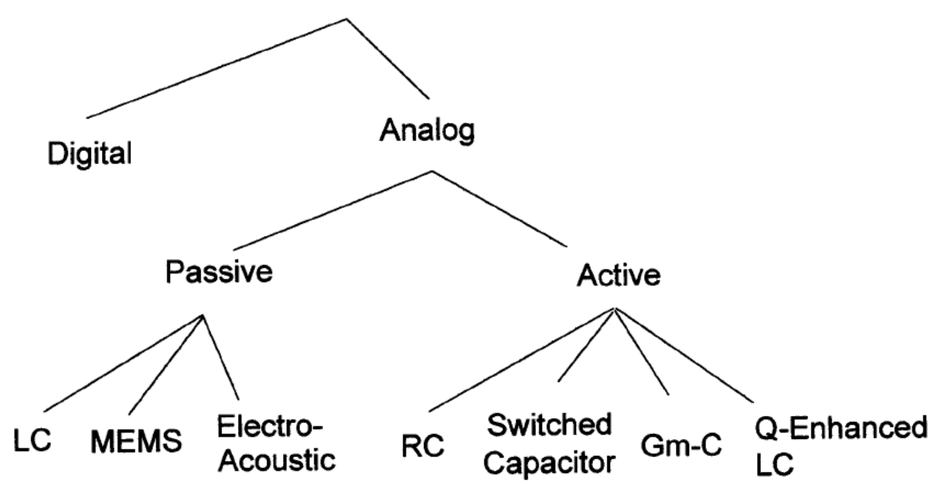


For a “narrowband” approximation, the s-domain poles and zeros simply become replicated at $\pm j\omega$ with a smaller unit circle of radius $1/2a$. To realize a wideband filter, use a cascade of highpass and lowpass filters.

Notes on Filter Transformations

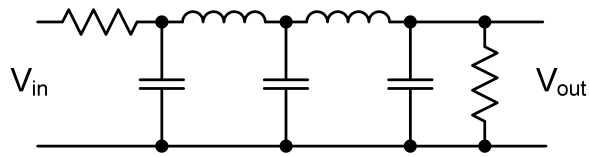
- This used to be a very important skill
- In the "old days" (before widespread use of computer tools) there were books filled with filter coefficients for lowpass prototypes
- As a designer, you then had to go and transform the filter into whichever other type you wanted
- Nowadays, we will directly synthesize the filter type we want
  - Using Matlab, Analog Filter Wizard, etc.

Filter Implementation Options



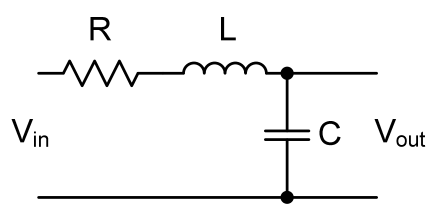
Filter Implementation Options

- It is possible to build arbitrary analog filters using RLC circuits
  – Example: "Ladder Filters"



- While this looks OK at first, we will typically want to avoid using inductors
  – Often big, bulky, expensive
- It turns out that we can also synthesize arbitrary filters without inductors, but with the help of active circuits, like opamps
- Many options exist, we'll look at two basic examples
  – State-space synthesis using opamps
  – Sallen-Key filters

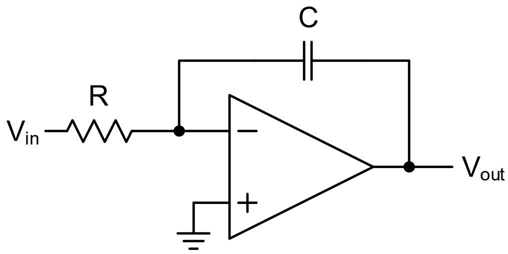
Starting Point: Passive LC Lowpass Filter



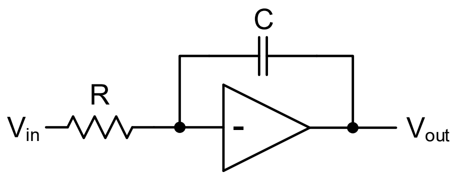
$$H(s) = \frac{\frac{1}{sC}}{\frac{1}{sC} + R + sL} = \frac{1}{1 + sRC + s^2LC} = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0{}^2}}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

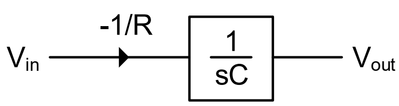
Opamp-Based Integrator



$$v_{out}(t) = -\frac{1}{C}\int \frac{v_{in}(t)}{R}dt$$

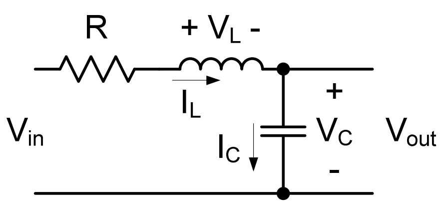


$$V_{out}(s) = -\frac{1}{sRC}V_{in}(s)$$



State-Space Filter Synthesis

State variables
(integrator outputs)



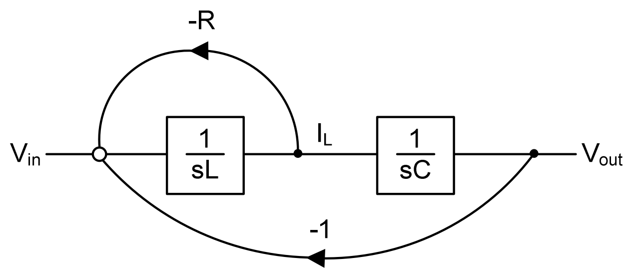
$$v_c(t) = \frac{1}{C}\int i_c(t)dt \qquad i_L(t) = \frac{1}{L}\int v_L(t)dt$$

$$V_c(s) = \frac{1}{sC}I_c(s) \qquad I_L(s) = \frac{1}{sL}V_L(s)$$

$$V_c = \frac{1}{sC}I_c = \frac{1}{sC}I_L = V_{out}$$

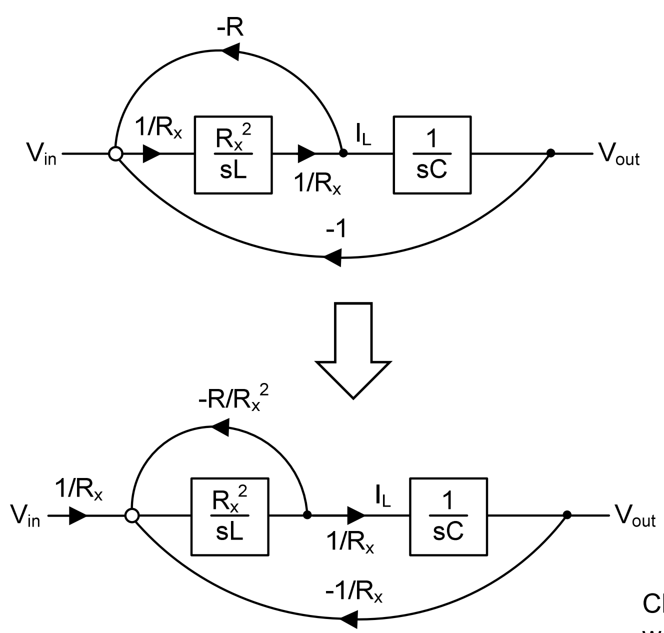
$$I_L = \frac{1}{sL}V_L = \frac{1}{sL}\left(V_{in} - I_L R - V_{out}\right)$$

Block Diagram



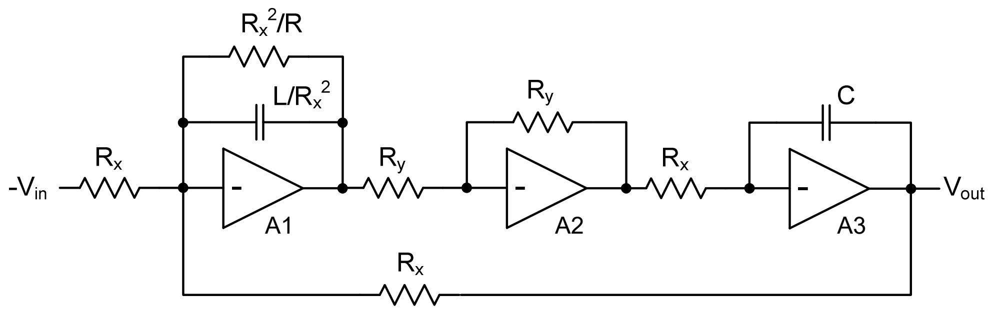
- Looks promising, but the problem with this realization is that the first integrator takes a voltage at the input and produces a current at the output
  - We need the opposite if we want to realize the circuit with an opamp integrator

Modified (Equivalent) Block Diagrams



Choice of R_x is arbitrary, we can simply make it equal to R

Implementation

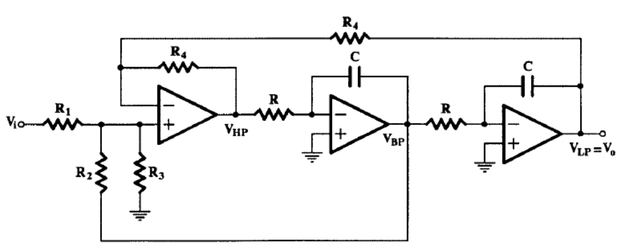


$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{1 + sRC + s^2LC}$$

- One remaining issue is that the transfer function is inverted
  - We could fix that (if needed) using a fourth op-amp

Biquads

- Biquads are fine-tuned versions of the state-space filter that we derived
- They allow us to implement arbitrary second order transfer functions with two poles and two zeros
- We can cascade biquads to realize filters of arbitrary order



W.J. Kerwin, L.P. Huelsman, R.W Newcomb, "State-Variable Synthesis for Insensitive Integrated Circuit Transfer Functions," *IEEE JSSC,* vol.2, no.3, pp. 87-92, Sep. 1967.

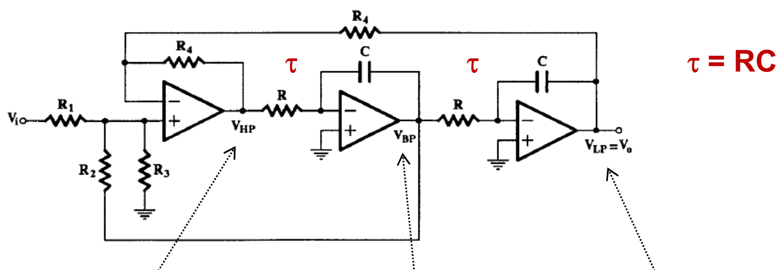
$$\omega_o = \frac{1}{RC} \qquad Q = \frac{R_1R_2 + R_1R_3 + R_2R_3}{2R_1R_3}$$

$$\frac{V_o}{V_i} = \frac{V_{LP}}{V_i} = \frac{K}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

$$K = \frac{2R_2R_3}{R_1R_2 + R_1R_3 + R_2R_3} = \frac{R_2}{R_1Q}$$

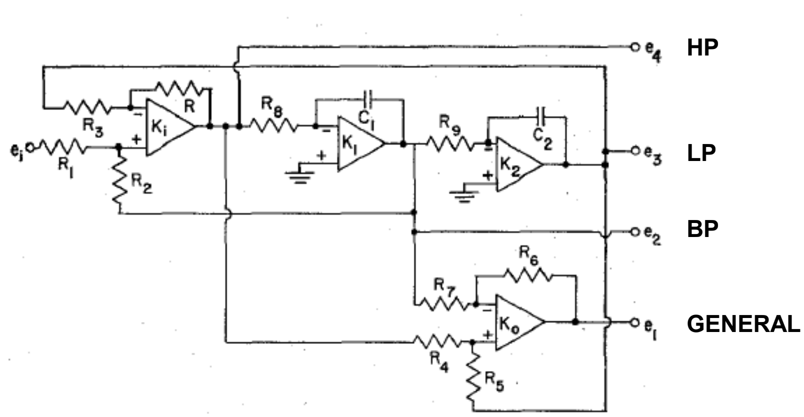
Highpass and Bandpass Output

- An interesting feature of some biquads is that they provide additional highpass and bandpass outputs for "free"



$$H_{HP}(s) = \frac{s^2\tau^2}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \qquad H_{BP}(s) = \frac{-s\tau}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \qquad H_{LP}(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

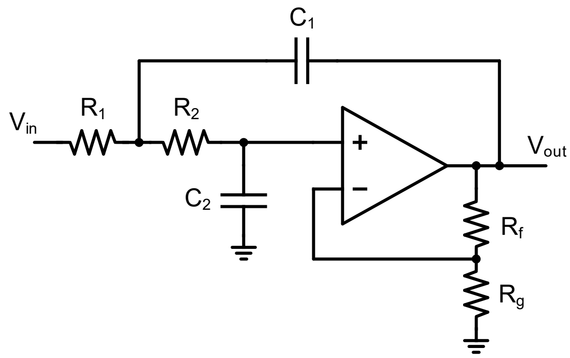
General Biquad



$$H_{GENERAL}(s) = \frac{b_2 s^2 + b_1 s + b_0}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

Implements arbitrary poles and zeros

Sallen-Key Lowpass Filter



$$K = \frac{R_f + R_g}{R_g}$$

$$H(s) = \frac{K}{1 + \frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p^2}}$$

$$\omega_p = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

$$Q_p = \frac{\omega_p}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-K}{R_2 C_2}}$$

- Single opamp
- Poles only, no zeros
- Similar circuits exist for HP, BP, etc.

State-Space Biquad or Sallen-Key?

- Suppose we wanted to realize a second-order filter with poles only
  - Should we use a Biquad or Sallen-Key realization?
- From a complexity perspective, we would obviously go for Sallen-Key
- But, the Sallen-Key circuit comes with a few potential disadvantages that may (or may not be) be a problem
  - Sensitivity to parasitic capacitance; this is less of an issue in a state-space circuit due its virtual ground nodes
  - Undesired tradeoff between component spread and sensitivity to component inaccuracy
  - Increased sensitivity to component inaccuracy for high-Q poles
- Let's take a closer look…

Definition of Sensitivity

- The sensitivity of any variable y to any parameter x is defined as

$$S_x^y = \lim_{\Delta x \to 0}\left(\frac{\Delta y / y}{\Delta x / x}\right) = \frac{x}{y}\lim_{\Delta x \to 0}\frac{\Delta y}{\Delta x} = \frac{x}{y}\frac{\partial y}{\partial x}$$

- In order to relate fractional changes in y to fractional changes in x we can then write

$$\frac{\Delta y}{y} \cong S_x^y \frac{\Delta x}{x}$$

- Example

$$S_x^y = 10 \qquad \frac{\Delta x}{x} = 2\% \qquad \Rightarrow \frac{\Delta y}{y} \cong 20\%$$

- Common sense: sensitivity is a first order approximation, accurate only for “small” errors

Parameter Variations of Discrete Components



- The best we can do on a printed circuit board
  - Metal film resistors are ~0.1% inaccurate, 5 ppm/°C
  - C0G dielectric capacitors, 2% inaccurate, very small temperature dependence
- Other, cheaper components show larger variations
- Bottom line: RC products can easily vary by a few percent

Sensitivity to Component Inaccuracy for a Sallen-Key LPF

$$\omega_P = \frac{1}{\sqrt{R_1C_1R_2C_2}}$$

$$Q_P = \frac{\omega_P}{\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-G}{R_2C_2}}$$

$$S_{R_1}^{\omega_P} = S_{R_2}^{\omega_P} = S_{C_1}^{\omega_P} = S_{C_2}^{\omega_P} = -\frac{1}{2}$$

$$S_{R_1}^{Q_P} = -S_{R_2}^{Q_P} = -\frac{1}{2} + Q_P\sqrt{\frac{R_2C_2}{R_1C_1}}$$

$$S_{C_1}^{Q_P} = -S_{C_2}^{Q_P} = -\frac{1}{2} + Q_P\left(\sqrt{\frac{R_1C_2}{R_2C_1}} + \sqrt{\frac{R_2C_2}{R_1C_1}}\right)$$

$$S_G^{Q_P} = Q_PG\sqrt{\frac{R_1C_1}{R_2C_2}}$$

- Sensitivity depends on Q_P and “component spread” i.e. the ratios of the resistors and capacitors, respectively

Example

- Want to design a Sallen-Key filter with Q_P=10
- Choice 1: All R and C are the same $\Rightarrow$ G = 3 -(1/Q_P) = 2.9
  - Very nice from the perspective of component spread, but bad for sensitivity, e.g.

$$S_{R_1}^{Q_P} = -\frac{1}{2} + Q_P = 9.5$$

- Choice 2: Reduce sensitivity by accepting large component spread
  - Can show that G=1 is a good choice
    - See e.g. http://www.maxim-ic.com/appnotes.cfm/an_pk/738
      - Note: The expression for S^Q_K is incorrect this application note (R_3 and R_1 should be interchanged in this expression to match the result on the previous slide)

- For G=1, we have

$$Q_P = \frac{\omega_P}{\dfrac{1}{R_1C_1} + \dfrac{1}{R_2C_1}}$$

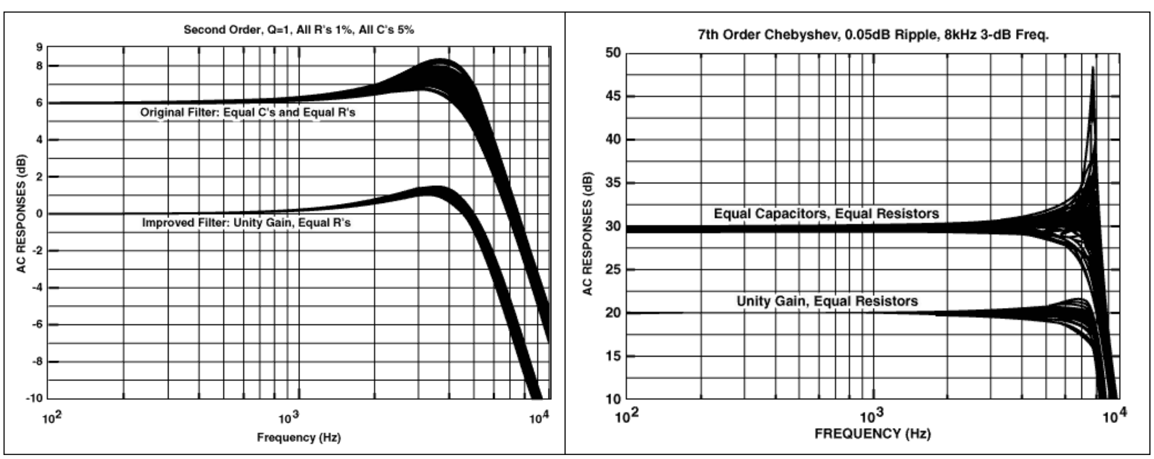
$$S_{R_1}^{Q_P} = -\frac{1}{2} + \frac{R_2}{R_1 + R_2} = 0 \qquad for \quad R_1 = R_2$$

- Unfortunately, in this case

$$\frac{C_1}{C_2} = 4Q_P^2 = 400 \qquad for \quad Q_P = 10$$

- Bottom line: The Sallen-Key realization suffers from a strong tradeoff between sensitivity and component spread

Case Studies



MAXIM APPLICATION NOTE 738
Minimizing Component-Variation Sensitivity in Single Op Amp Filters
http://www.maxim-ic.com/appnotes.cfm/an_pk/738/

Summary

- Practical filter design is based on choosing a proper filter template (Butterworth, Bessel, etc.) and mapping the resulting poles and zeros into hardware
- While we can in principle build arbitrary filters using passive RLC circuits, we typically want to avoid inductors and instead use active circuits to achieve the desired mapping
- Sallen-Key implementations
  - Low complexity → Good for board level design
  - Undesired tradeoffs between pole Q, component spread and sensitivity
- State-space Biquads
  - Are known to be less sensitive, at the expense of increased complexity → This is OK for integrated circuits that anyway contain millions (or billions!) of transistors

Chapter 18

Circuit Simulation

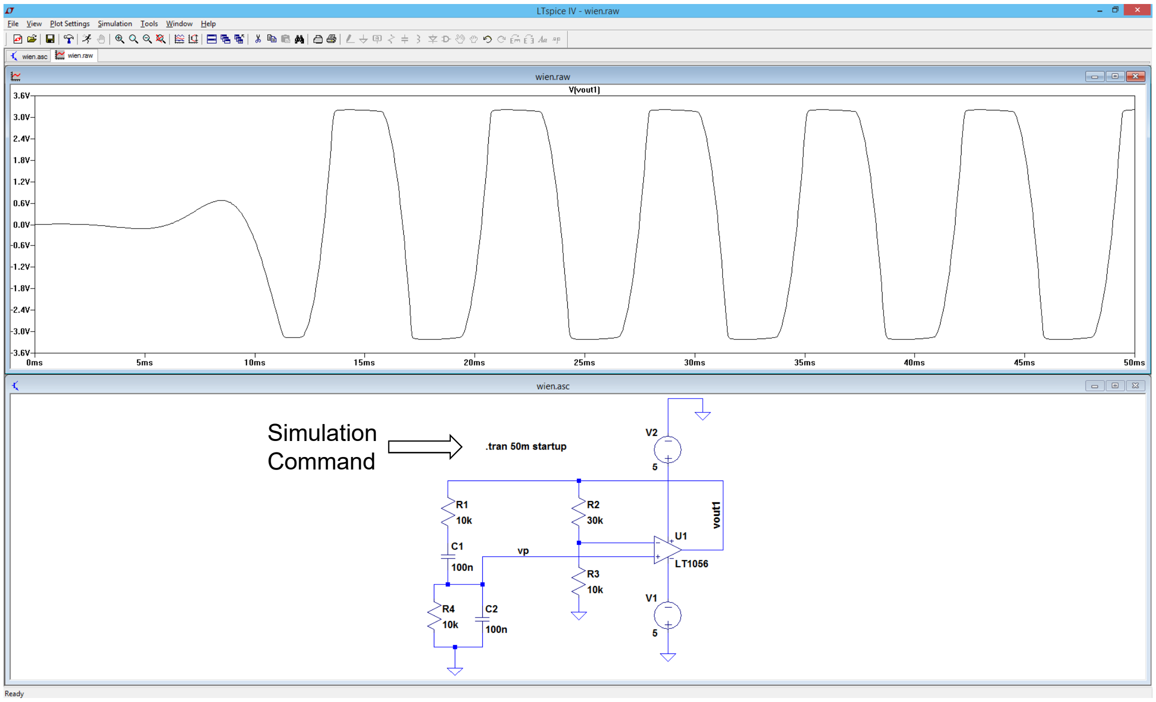
Boris Murmann

Stanford University

SPICE

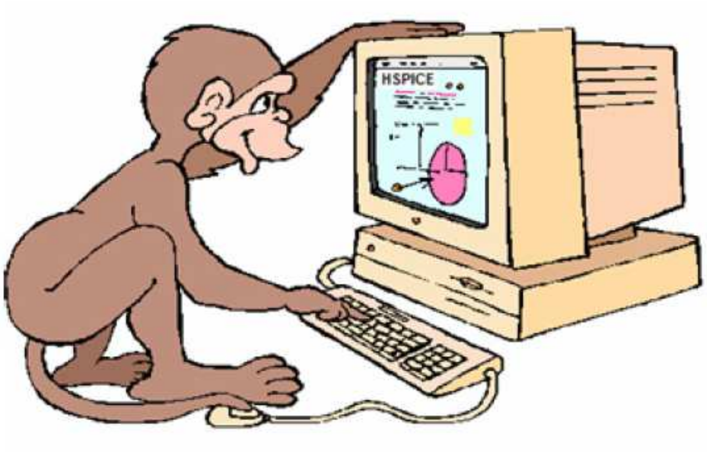
- SPICE stands for Simulation Program with Integrated Circuit Emphasis
- SPICE simulates the behavior of circuits by numerically solving the pertaining set of equations
  - Really just a gigantic calculator
- The original version of SPICE originated at UC Berkeley in the 1970s
- Information about the history of SPICE can be found at
  - http://www.coe.berkeley.edu/labnotes/0502/history.html
  - http://www.ecircuitcenter.com/SpiceTopics/History.htm
- SPICE webpage at UC Berkeley
  - http://bwrc.eecs.berkeley.edu/Classes/IcBook/SPICE
- Dozens of different versions available today
  - PSpice, HSpice, Eldo, Spectre, LTSpice, NGSpice, ICircuit, …
- In this class, we will use LTSpice
  - Download at www.linear.com/ltspice

LTSpice Window



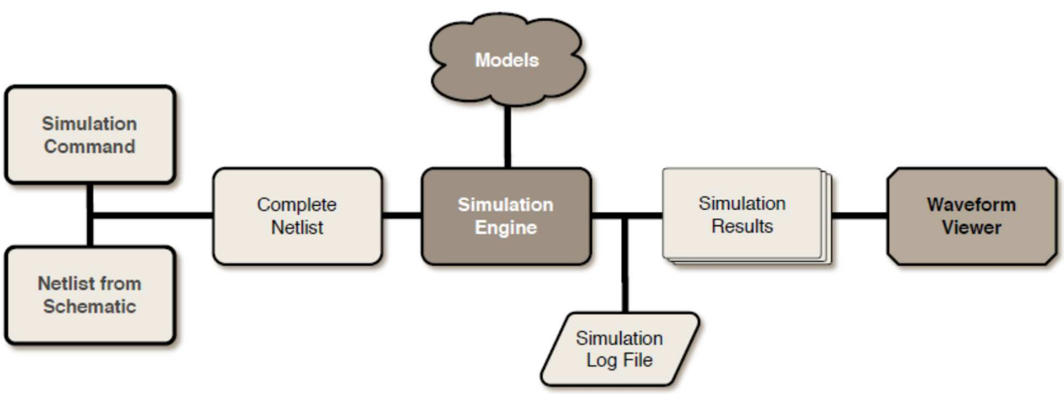
- SPICE won't "think" for you
  - It's really just a tool for crunching the numbers much faster than you can
- How to properly use SPICE?
  - First, design the circuit using "your head"
    - Understand how the circuit works, what is important, what is a first order effect, second order effect, etc.
    - Use hand calculations, computer programs like Excel or MATLAB, to find initial component values and performance estimates
  - Simulate your hand design with SPICE and inspect the result
    - If your prediction and SPICE's answer differ, question your hand calculations and question SPICE
  - Perform final tweaks with SPICE
    - SPICE can help you take into account effects that you can't analyze with simple hand analysis (e.g. high frequency poles)
- How not to use SPICE?
  - Guess some random component sizes and simulate in SPICE
  - Iterate until the circuit somehow does what you want

SPICE Monkey



[Courtesy Isaac Martinez]

Structure of a Circuit Simulator

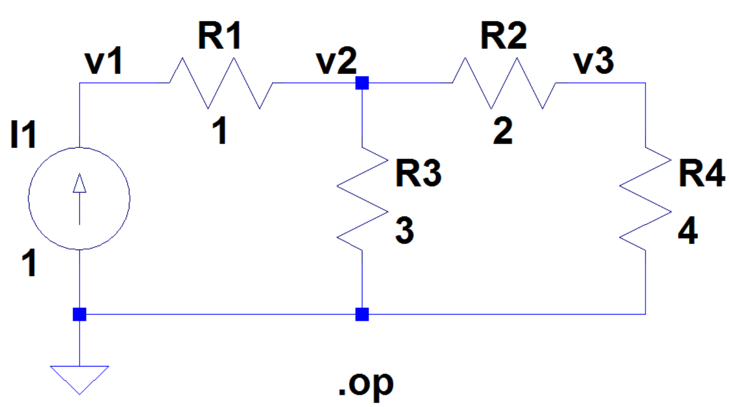


[Maloberti, Chapter 1]

Basic Analysis Modes

- OP Analysis
  - Compute the DC operating point of a circuit
- DC Analysis
  - Similar to operating point analysis, but we can sweep certain parameters. For example, sweep the input voltage to find the large signal transfer characteristic. Capacitors are open circuits, inductors are shorts.
- AC Analysis
  - Computes the frequency response of a circuit based on its operating point parameters. The circuit is linearized at the operating point in the same way we do in this in hand analysis
- Transient Analysis
  - This is analogous to building the circuit in the lab and observing the signals of interest over time on an oscilloscope.

Example 1 (OP)



Netlist

```
R1  v1   v2    1
R2  v2   v3    2
R4  v3   0     4
I1   0   v1    1
R3  v2   0     3
.op
.backanno
.end
```

- For more details on SPICE netlist syntax, refer to http://www.ecircuitcenter.com/Basics.htm

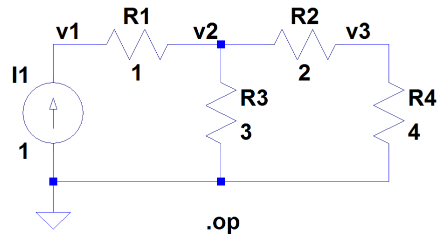
Result

```
* C:\Users\murmann\Box Sync\teaching\EE101B\ee101b_spring_2014\ltspice\Draft1.asc

       --- Operating Point ---

V(v1):         3            voltage
V(v2):         2            voltage
V(v3):         1.33333      voltage
I(I1):         1            device_current
I(R3):         0.666667     device_current
I(R4):         0.333333     device_current
I(R2):         0.333333     device_current
I(R1):         1            device_current
```

Under the Hood

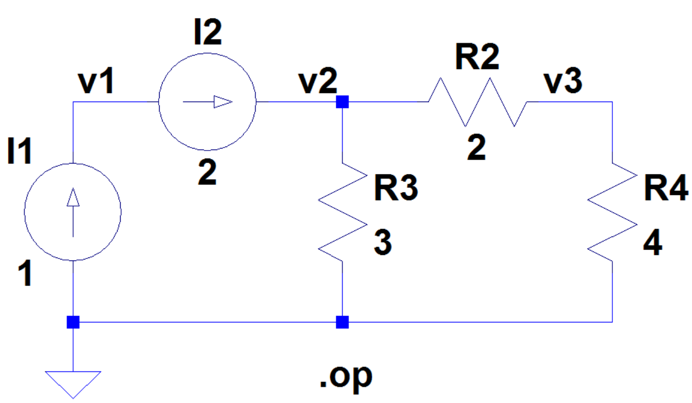
- In this example, SPICE simply solves a linear system of equations
  - Think Gaussian elimination, done numerically

$$0 = -I_1 + \frac{V_1 - V_2}{R_1}$$
$$0 = \frac{V_2 - V_1}{R_1} + \frac{V_2}{R_3} + \frac{V_2 - V_3}{R_2}$$
$$0 = \frac{V_3 - V_2}{R_2} + \frac{V_3}{R_4}$$

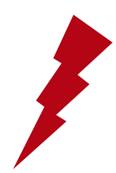


$$\begin{bmatrix} \frac{1}{R_1} & -\frac{1}{R_1} & 0 \\ -\frac{1}{R_1} & \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} & -\frac{1}{R_2} \\ 0 & -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ 0 \\ 0 \end{bmatrix} \qquad \begin{bmatrix} 1 & -1 & 0 \\ -1 & \frac{11}{6} & -\frac{1}{2} \\ 0 & -\frac{1}{2} & \frac{3}{4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$

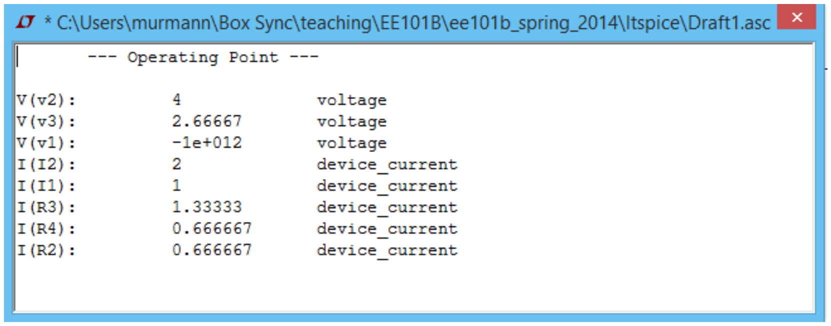
This Should Not Work…



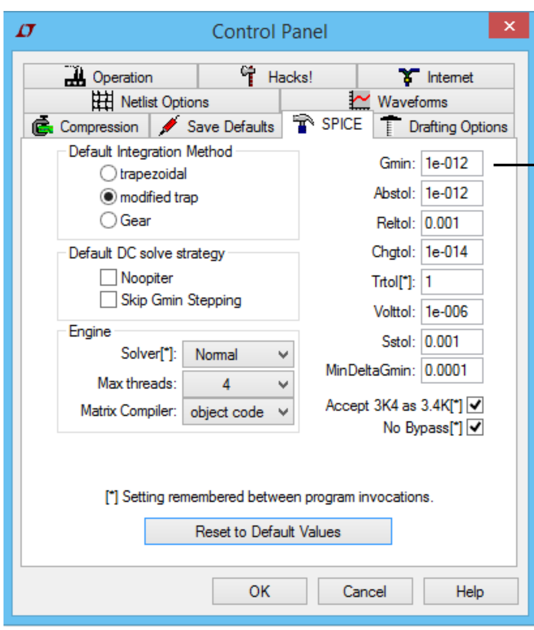
$$0 = -I_1 + I_2 \qquad 0 = -1 + 2$$



But it Does!



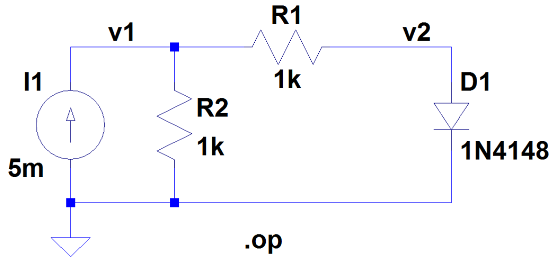
- -1 teravolts at node V1
- What's going on?

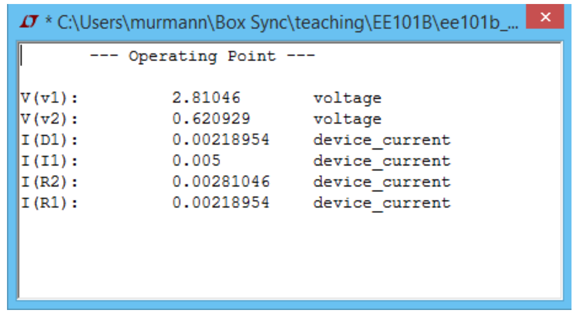


The tool automatically inserts a conductance of 1pS at each node; this helps the tool to "converge" even when there are "floating" nodes

- Key take-home
  - Numerical tools behave "funny" when you ask them dumb questions
  - Garbage in → garbage out
- If something strange comes out of SPICE, chances are that you have made a mistake, and the tool is just trying to do its best…

Example 2 (OP)






```
       --- Operating Point ---

V(v1):          2.81046         voltage
V(v2):          0.620929        voltage
I(D1):          0.00218954      device_current
I(I1):          0.005           device_current
I(R2):          0.00281046      device_current
I(R1):          0.00218954      device_current
```

- This is a nonlinear circuit, so linear algebra alone won't do the trick
- How does SPICE get the answer?

- We can still describe the circuit in matrix format

$$\begin{bmatrix} 2m & -1m \\ -1m & 1m \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 5m \\ -\left(e^{\frac{V_2}{V_T}} - 1\right) \end{bmatrix}$$

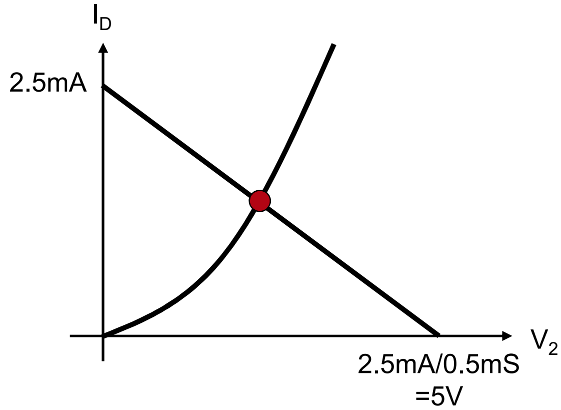
- And we can perform Gaussian elimination to make the conductance matrix triangular

$$\begin{bmatrix} 2m & -1m \\ 0 & 0.5m \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 5m \\ -I_s\left(e^{\frac{V_2}{V_T}} - 1\right) + 2.5m \end{bmatrix}$$

- Next steps
  - Solve the transcendental equation in V_2
  - Then back substitute as usual to get V_1

Solving the Transcendental Equation

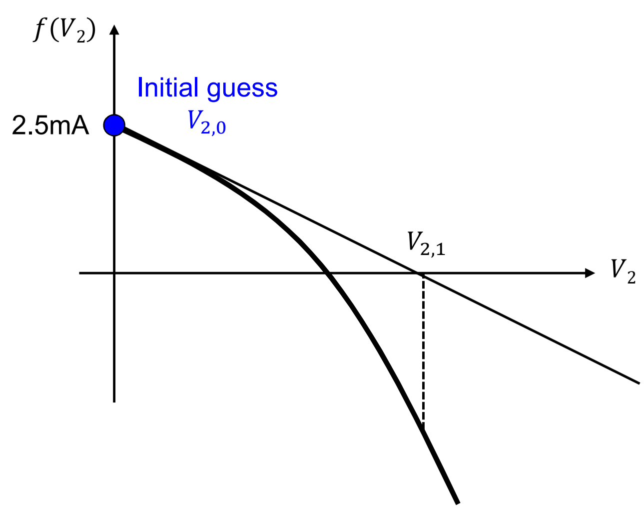
$$0.5m \cdot V_2 = -I_s\left(e^{\frac{V_2}{V_T}} - 1\right) + 2.5m \qquad 2.5m - 0.5m \cdot V_2 = I_s\left(e^{\frac{V_2}{V_T}} - 1\right)$$



- We need to find the intersect of the two curves
- SPICE does this using Newton-Raphson iterations

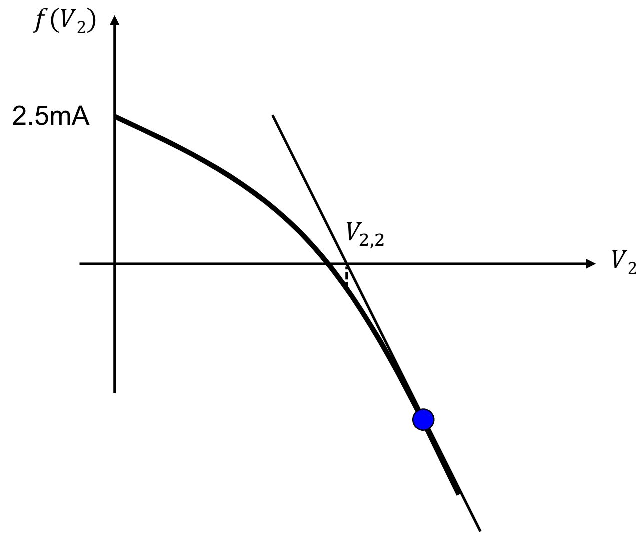
$$f(V_2) = 2.5m - 0.5m \cdot V_2 - I_s\left(e^{\frac{V_2}{V_T}} - 1\right)$$

$$V_{2,n+1} = V_{2,n} - \frac{f\left(V_{2,n}\right)}{f'\left(V_{2,n}\right)}$$



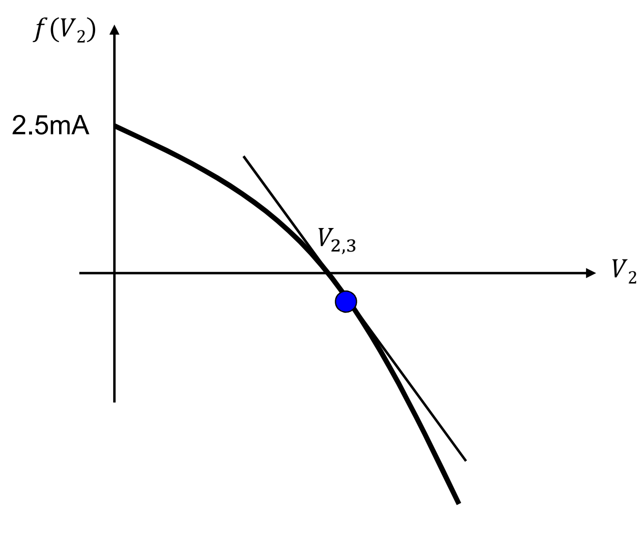
$$f(V_2) = 2.5m - 0.5m \cdot V_2 - I_s\left(e^{\frac{V_2}{V_T}} - 1\right)$$

$$V_{2,n+1} = V_{2,n} - \frac{f\left(V_{2,n}\right)}{f'(V_{2,n})}$$

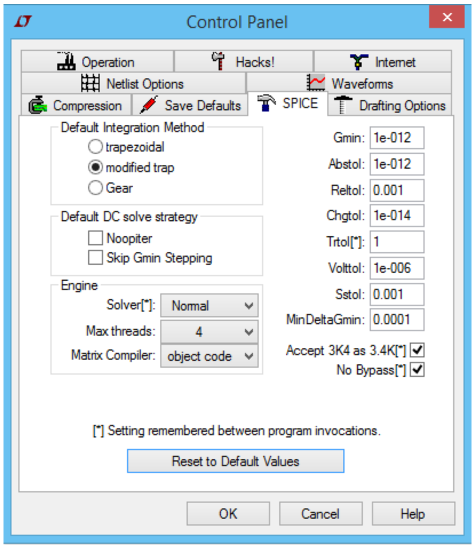


$$f(V_2) = 2.5m - 0.5m \cdot V_2 - I_s\left(e^{\frac{V_2}{V_T}} - 1\right)$$

$$V_{2,n+1} = V_{2,n} - \frac{f\left(V_{2,n}\right)}{f'(V_{2,n})}$$



- If the function f is well behaved, we can get arbitrarily close to the true solution of the transcendental equation
  - But we obviously want to stop at some point

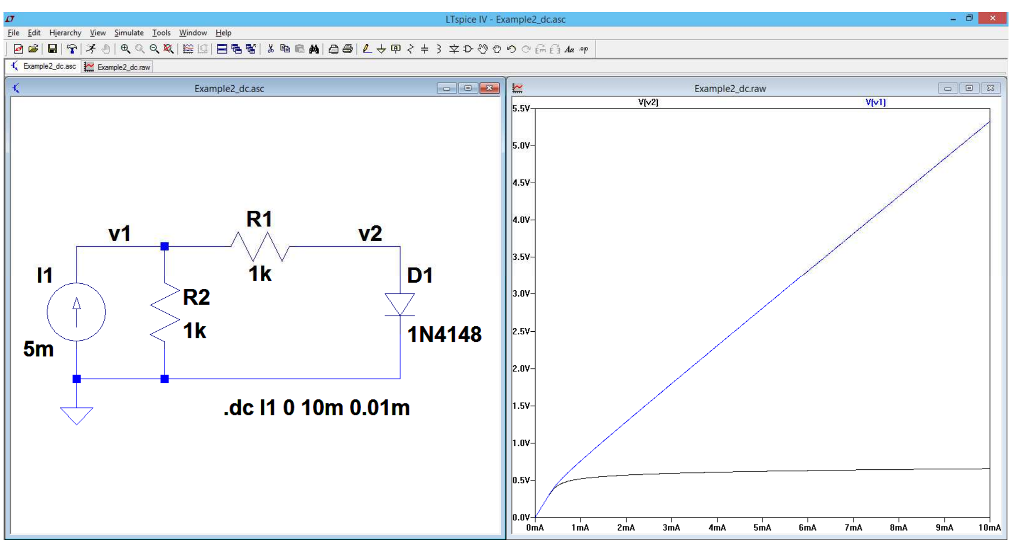


The Newton-Raphson iterations end when these error tolerances are met

See SPICE manual or advanced books if you are curious about what these settings mean

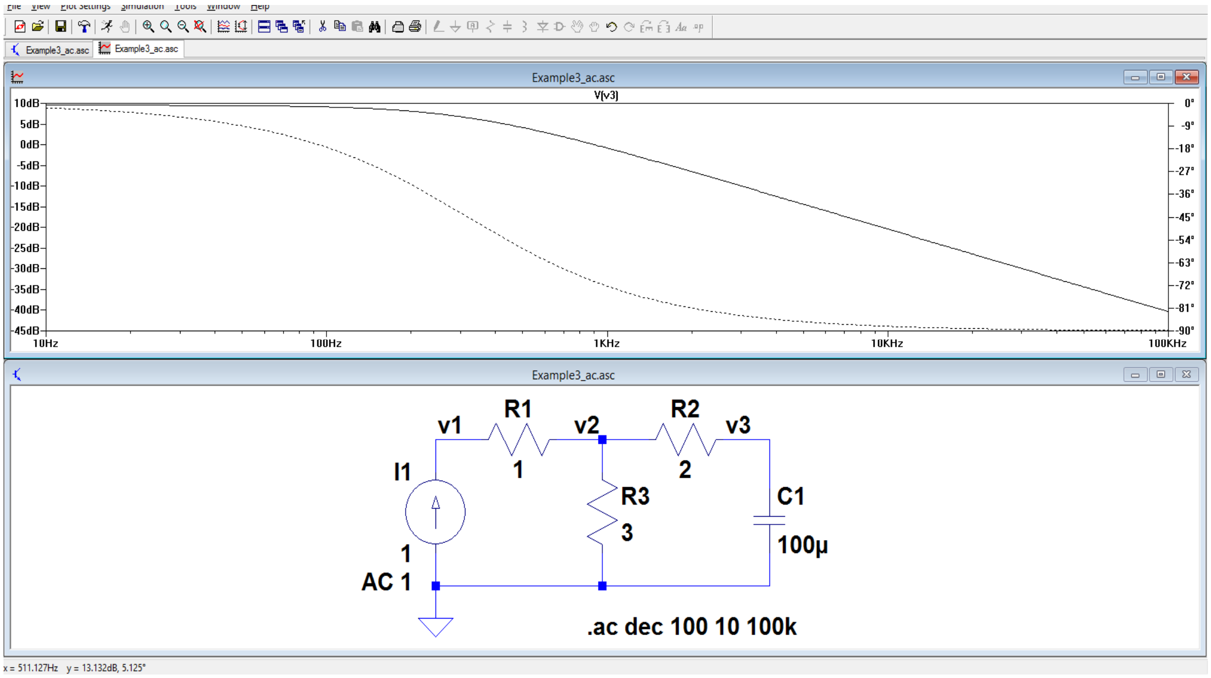
If the simulation does not converge, changing these settings may help

Example 3 (DC)



- In this example, the input source is swept and essentially an operating point analysis is performed in each step
  - Result from previous step comes in handy as initial guess for Newton-Raphson iterations

Example 4 (AC)

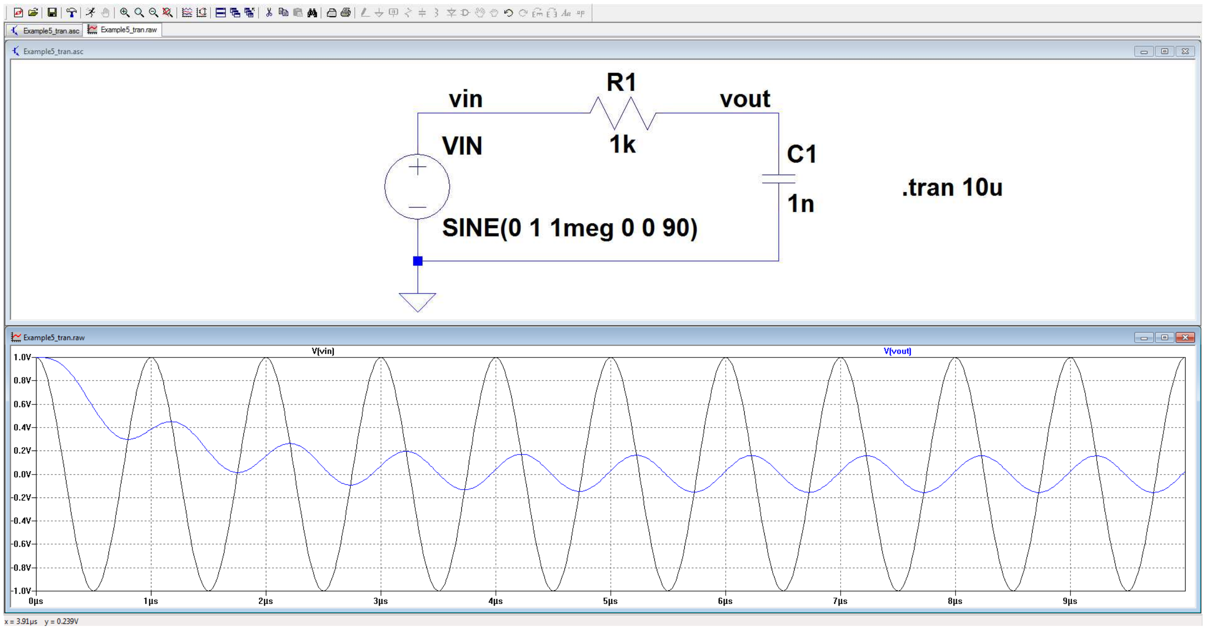


What Happens During AC Analysis?

$$\begin{bmatrix} \frac{1}{R_1} & -\frac{1}{R_1} & 0 \\ -\frac{1}{R_1} & \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3} & -\frac{1}{R_2} \\ 0 & -\frac{1}{R_2} & \frac{1}{R_2}+j\omega C_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ 0 \\ 0 \end{bmatrix} \qquad \begin{bmatrix} 1 & -1 & 0 \\ -1 & \frac{11}{6} & -\frac{1}{2} \\ 0 & -\frac{1}{2} & \frac{3}{4}+j\omega\cdot 100\mu \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$

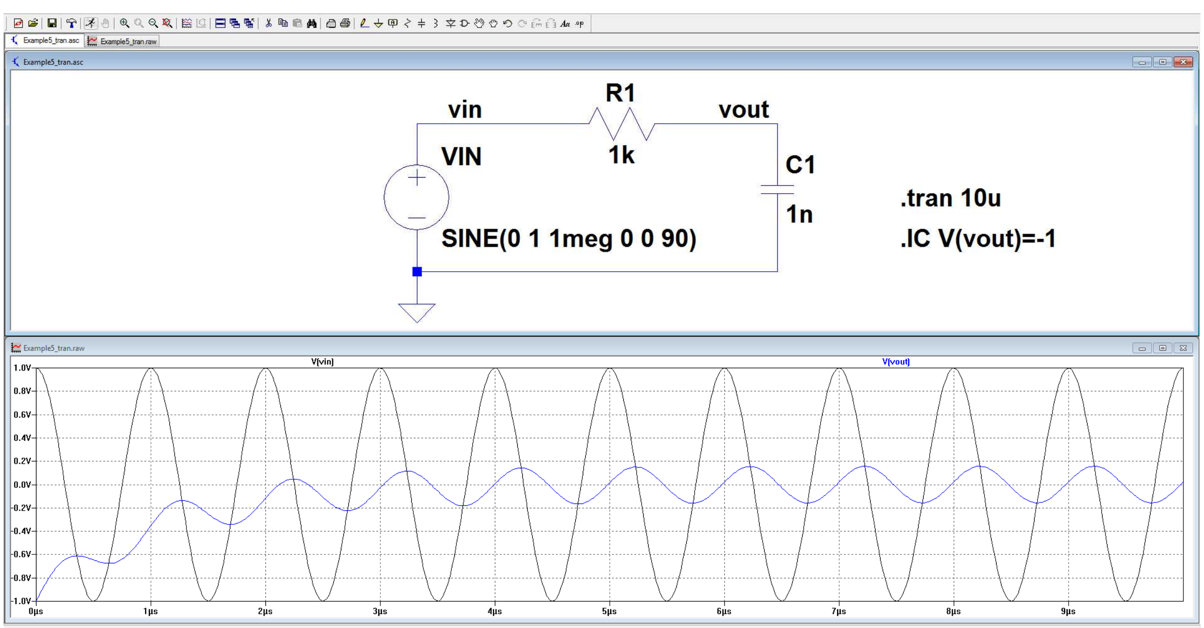
- Again just linear algebra, as in the operating point analysis with linear elements (example 1)
- But, this time with complex numbers, and with ω as a parameter
- The statement "`.ac dec 100 10 100k`" tells SPICE to
  - Perform a logarithmix sweep in frequency with 100 points per decade
  - Start at 10 Hz and end at 100 kHz
  - Means that the tool solves 100·4 = 400 complex matrix equations to generate the plot on the previous slide

Example 5 (TRAN)

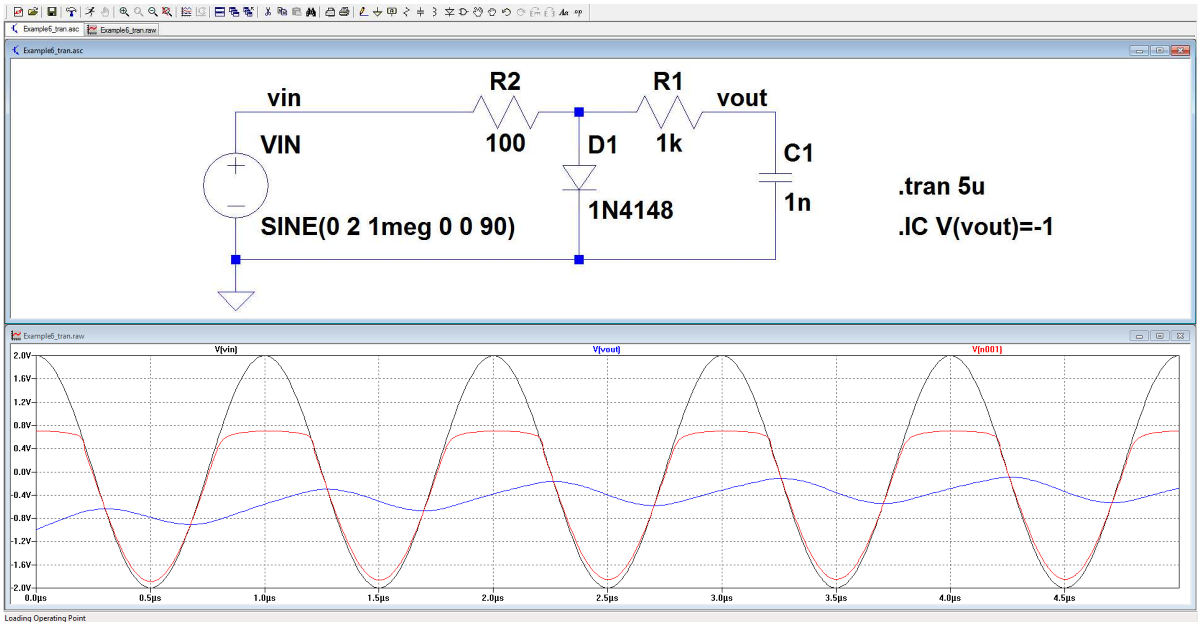


Specifying Initial Conditions

- Unless we specify an initial condition, Spice assumes that the initial voltage across the capacitor is the same as the applied input at t=0 (see previous slide)

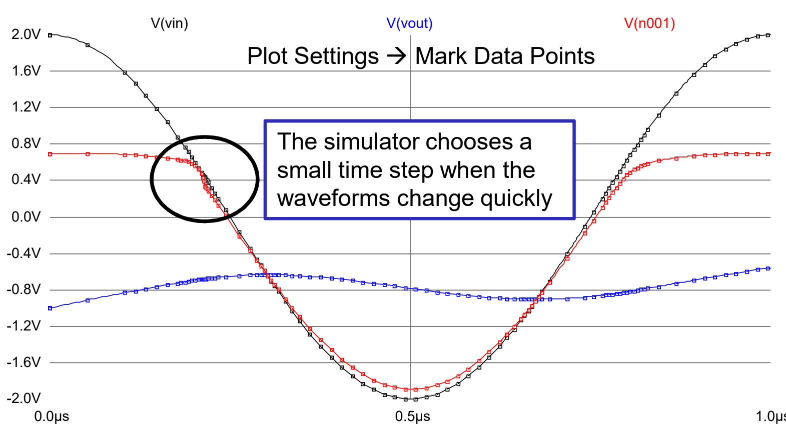


Example 6 (TRAN)



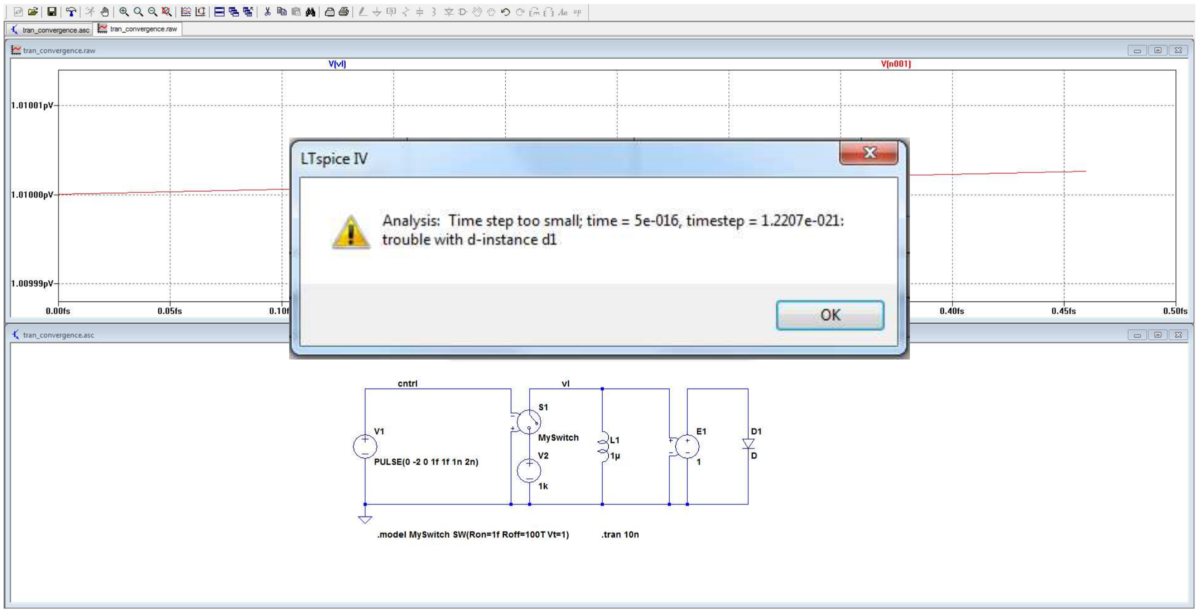
Under the Hood of Transient Analysis

- Transient analysis is the most complex among the analysis types we have discussed
- The simulator solves the circuit's system of nonlinear differential equations numerically and at discrete time instances
  - Think Newton-Raphson, but with numerical integration in time to take the behavior of energy storage elements into account

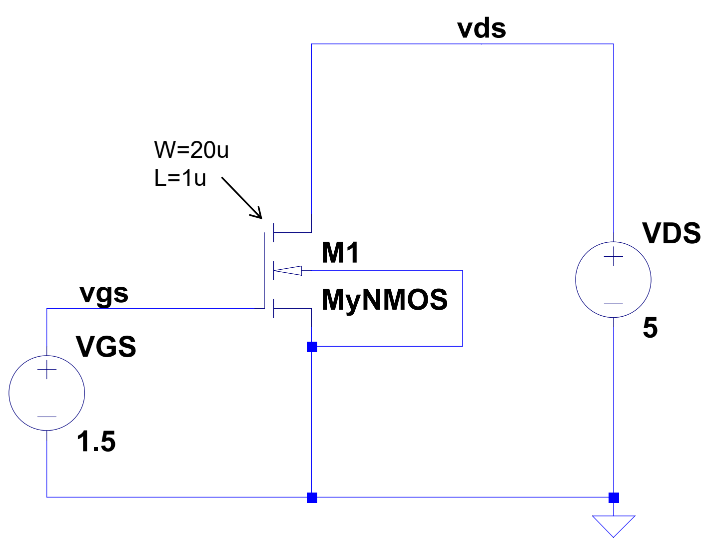


Transient Analysis Convergence Problems

- Non-convergence during transient analysis is usually related to extreme derivatives or discontinuities, often caused by bad component models or unreasonable circuits



Simulating MOSFET Circuits



.MODEL MyNMOS NMOS (KP=50u VT0=0.5) MOSFET parameters

.dc VDS 0 5 0.01 VGS 1 5 0.5 Two-dimensional DC sweep

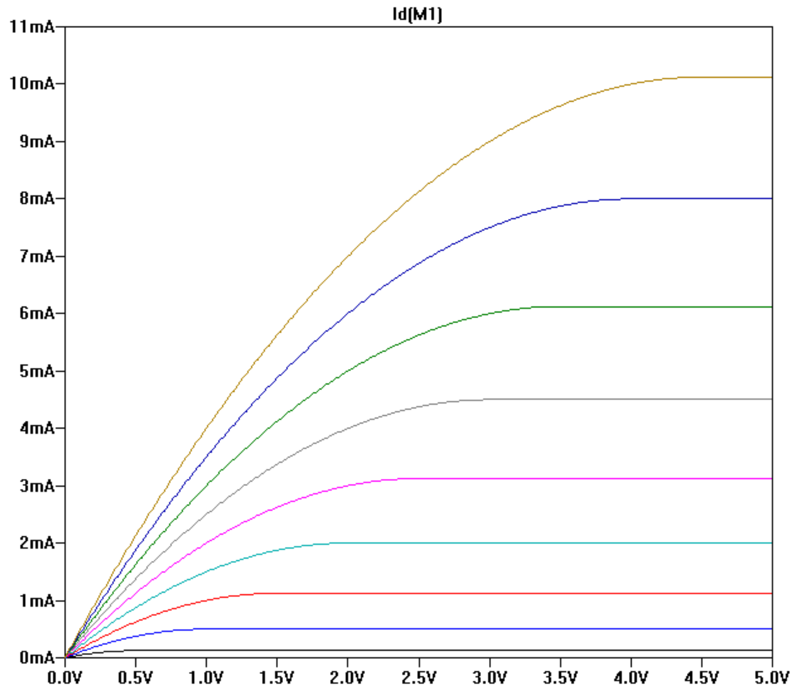
Level 1 MOSFET Model

Name	Description	Units	Default	Example
Vto	Zero-bias threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V^2	2e-5	3e-5
Gamma	Bulk threshold parameter	$V^{1/2}$	0.	0.37
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation (level 1 and 2 only)	1/V	0.	0.02
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Cbd	Zero-bias B-D junction capacitance	F	0.	20f
Cbs	Zero-bias B-S junction capacitance	F	0.	20f
Is	Bulk junction saturation current	A	1e-14	1e-15
N	Bulk diode emission coefficient	-	1.	
Pb	Bulk junction potential	V	0.8	0.87

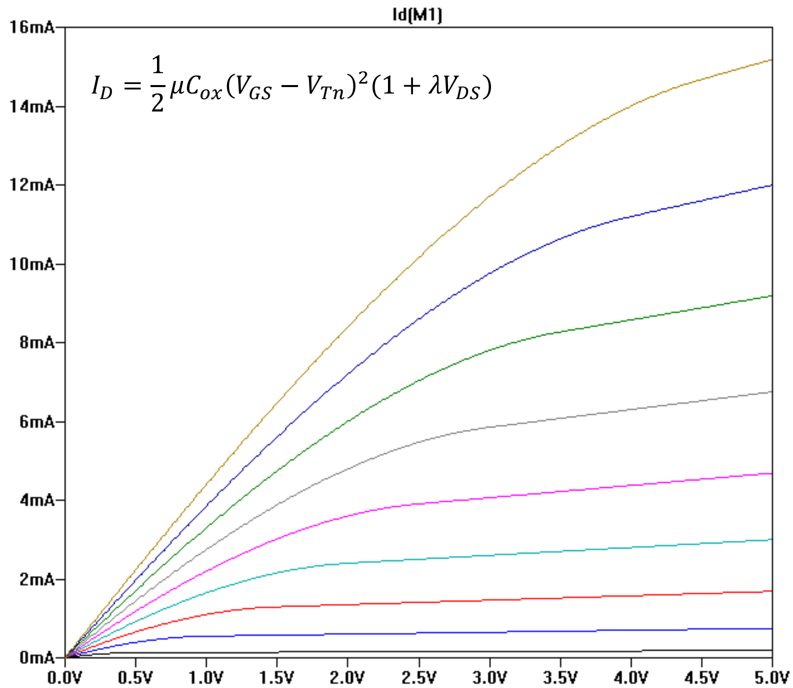
http://ltwiki.org/LTspiceHelp/LTspiceHelp/M_MOSFET.htm

Name	Description	Units	Default	Example
Cgso	Gate-source overlap capacitance per meter channel width	F/m	0.	4e-11
Cgdo	Gate-drain overlap capacitance per meter channel width	F/m	0.	4e-11
Cgbo	Gate-bulk overlap capacitance per meter channel width	F/m	0.	2e-10
Rsh	Drain and source diffusion sheet resistance	Ω	0.	10.
Cj	Zero-bias bulk junction bottom capacitance per square meter of junction area	F/m^2	0.	2e-4
Mj	Bulk junction bottom grading coefficient	-	0.5	0.5
Cjsw	Zero-bias bulk junction sidewall capacitance per meter of junction perimeter	F/m	0.	1p
Mjsw	Bulk junction sidewall grading coefficient	-	.50 level 1 .33 level 2,3	
Js	Bulk junction saturation current per square-meter of junction area	A/m	0.	1e-8
Tox	Oxide thickness	m	1e-7	1e-7
Nsub	Substrate doping	$1/cm^3$	0.	4e15

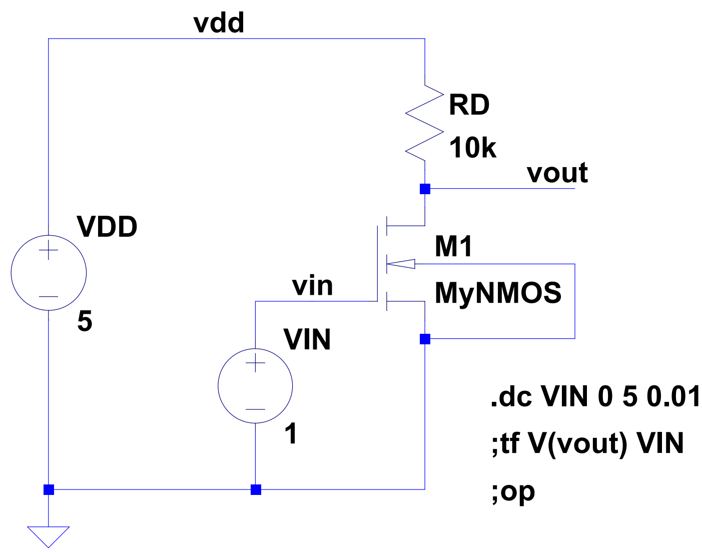
DC Sweep Results



Setting LAMBDA = 0.1



Example: CS Stage



.MODEL MyNMOS NMOS (KP=50u VT0=0.5)

Log File (OP Analysis)

```
Instance "m1": Length shorter than recommended for a level 1 MOSFET.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:          m1
Model:       mynmos
Id:          1.25e-04
Vgs:         1.00e+00
Vds:         3.75e+00
Vbs:         0.00e+00
Vth:         5.00e-01
Vdsat:       5.00e-01
Gm:          5.00e-04
Gds:         0.00e+00
Gmb:         0.00e+00
Cbd:         0.00e+00
Cbs:         0.00e+00
Cgsov:       0.00e+00
Cgdov:       0.00e+00
Cgbov:       0.00e+00
Cgs:         0.00e+00
Cgd:         0.00e+00
Cgb:         0.00e+00
```

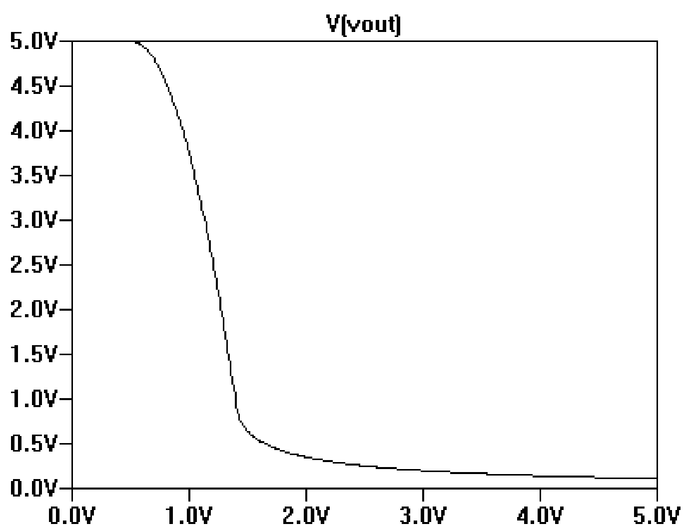
⇨ Can compare these numbers to hand analysis

TF Analysis Output

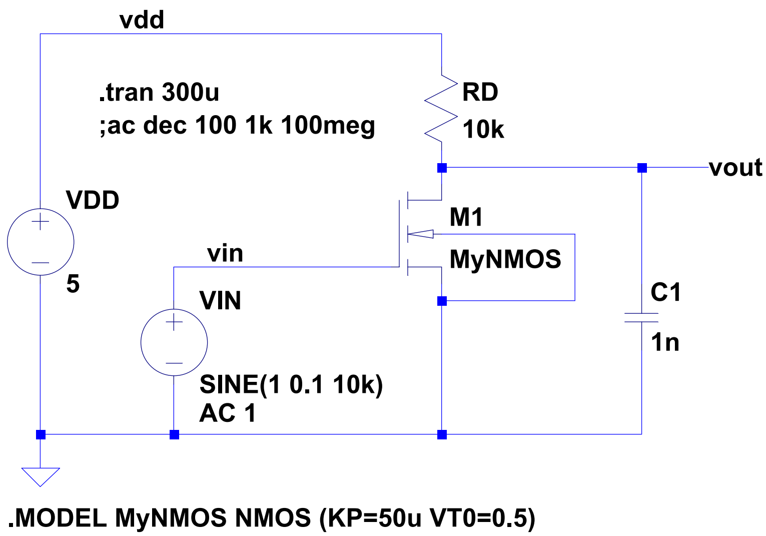
- Computes the small-signal gain and port impedances at the circuit's operating point

```
--- Transfer Function ---

Transfer_function:                  -5          transfer
vin#Input_impedance:                1e+020      impedance
output_impedance_at_V(vout):        10000       impedance
```


DC Sweep Output

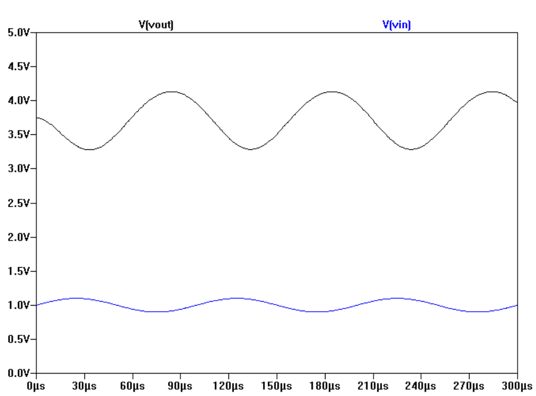


Transient and AC Simulation Example

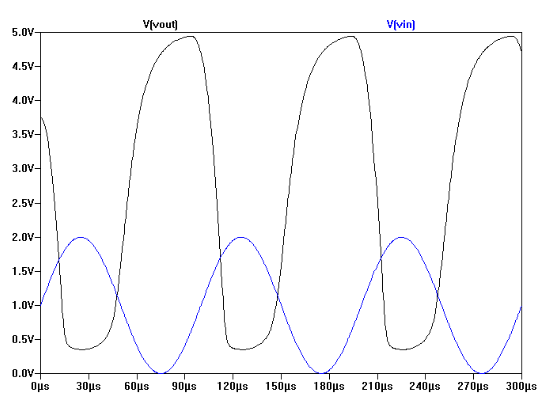


Transient Analysis Output

Input amplitude set to 100 mV

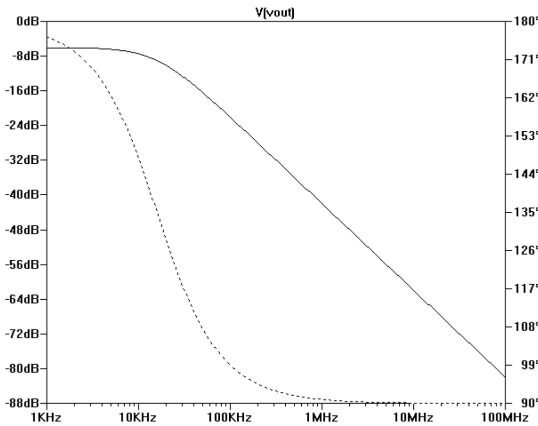


Input amplitude set to 1 V



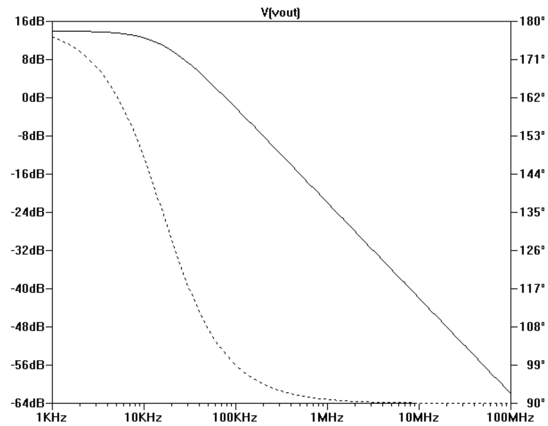
AC Analysis Output

AC Input amplitude set to 100 mV (-20 dBV)



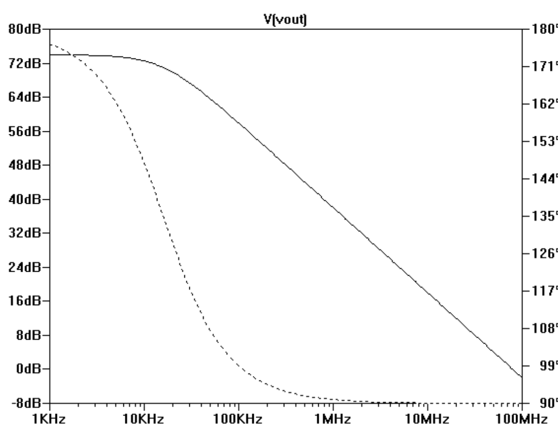
DC Gain = -6dBV – (-20dBV) = 14dB

AC Input amplitude set to 1 V (0 dBV)



DC Gain = 14dBV – 0dBV = 14dB

AC Input amplitude set to 1 kV (60 dBV)



DC Gain = 74dBV – 60dBV = 14dB

- Key Point: AC simulations are based on a linear circuit model; it does not matter which value we use for the AC input amplitude
- May as well set it to 1, in which case plotting the output is equivalent to plotting the circuit’s transfer function

Chapter 19

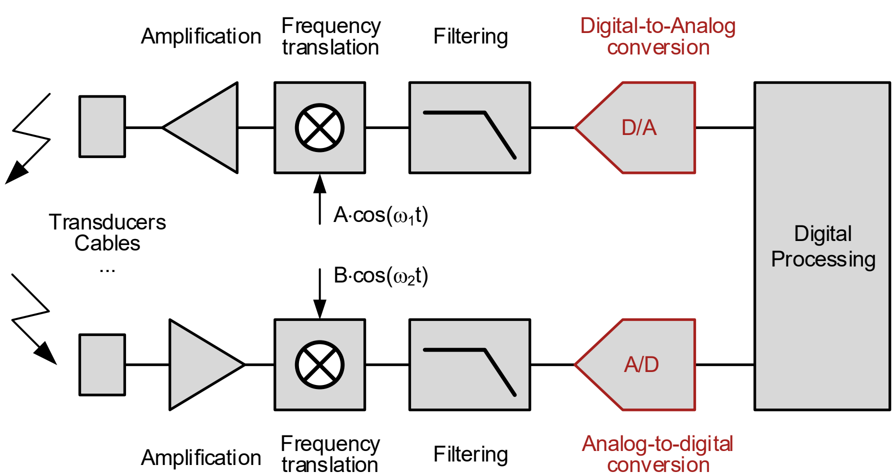
A/D and D/A Conversion

Boris Murmann

Stanford University

References:
Maloberti, Chapter 7
Analog Devices, The Data Conversion Handbook, Chapter 3

Motivation



- In almost all modern electronic systems, the information of interest is processed and/or stored in the digital domain
- This means that most systems need data converters (A/D and D/A)

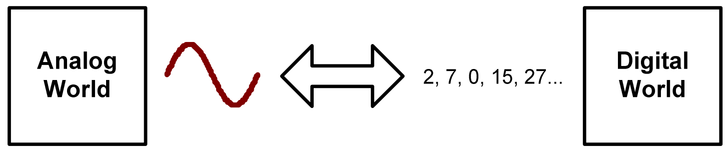
Data Converter Applications (1)

- Consumer electronics
  - Audio, TV, Video
  - Digital Cameras
  - Automotive control
  - Appliances
  - Toys
- Communications
  - Mobile Phones
  - Wireless Base Stations
  - Routers
  - Cable Tuners
  - Satellite Receivers

Data Converter Applications (2)

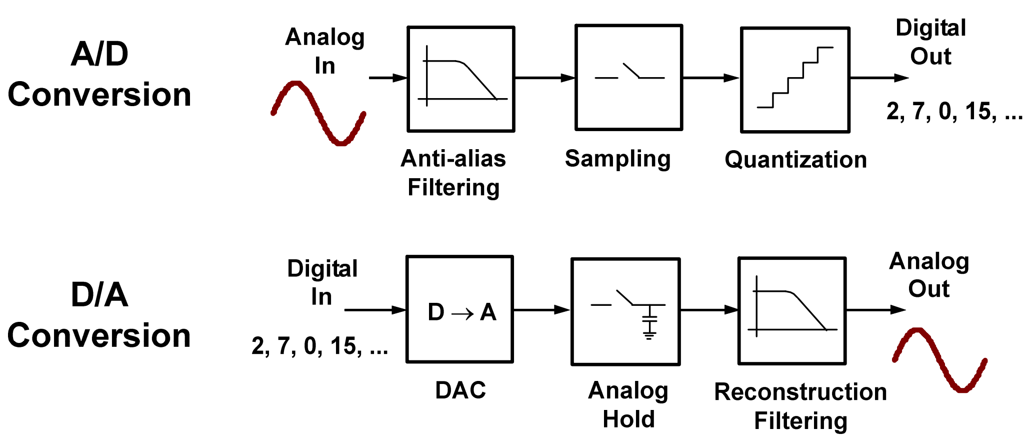
- Computing and Control
  - Storage media
  - Sound Cards
  - Data acquisition cards
- Instrumentation
  - Lab bench equipment
  - Semiconductor test equipment
  - Scientific equipment
  - Medical equipment

The Data Conversion Problem



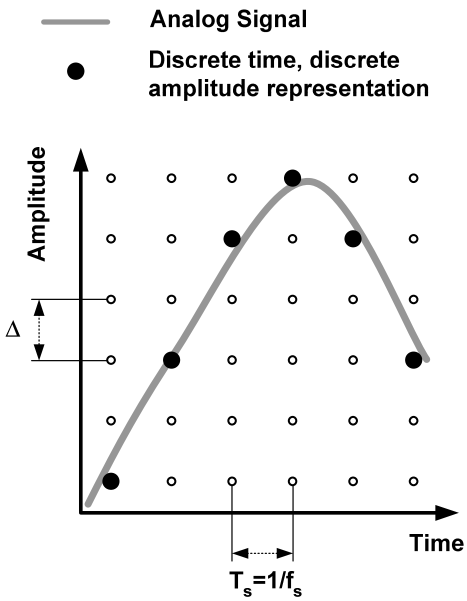
- Real world analog signals
  - Continuous time, continuous amplitude
- Digital abstraction
  - Discrete time, discrete amplitude
- Two problems
  - How to discretize in time and amplitude
    - A/D conversion
  - How to "undescretize" in time and amplitude
    - D/A conversion

Overview



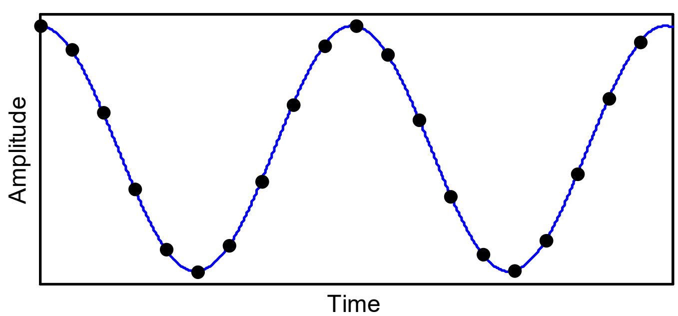
- We'll fist look at these building blocks from a functional, "black box" perspective
- Look at implementations later

Uniform Sampling and Quantization



- Most common way of performing A/D conversion
  - Sample signal uniformly in time
  - Quantize signal uniformly in amplitude
- Questions
  - How fast do we need to sample to preserve the information
  - How can we reconstruct the signal back into analog form?
  - How much "noise" is added due to amplitude quantization?
    - We will at first ignore amplitude quantization and come back to this later…

Sampling a Sinusoid



$$f_s = \frac{1}{T_s} = 1000kHz$$

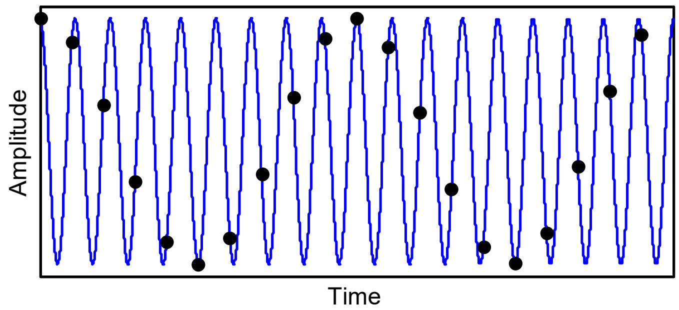
$$f_{sig} = 101kHz$$

$$v_{sig}(t) = cos(2\pi \cdot f_{in} \cdot t) \Rightarrow v_{sig}(n) = cos\left(2\pi \cdot \frac{f_{in}}{f_s} \cdot n\right)$$

$$\boxed{t \rightarrow n \cdot T_s = \frac{n}{f_s}}$$

$$= cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

f_{sig} changed to 899 kHz

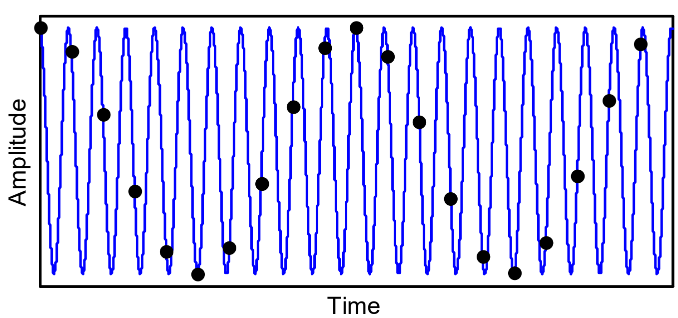


$$f_s = \frac{1}{T_s} = 1000kHz$$

$$f_{sig} = 899kHz$$

$$v_{sig}(n) = cos\left(2\pi \cdot \frac{899}{1000} \cdot n\right) = cos\left(2\pi \cdot \left[\frac{899}{1000} - 1\right] \cdot n\right) = cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

f_{sig} changed to 1101 kHz

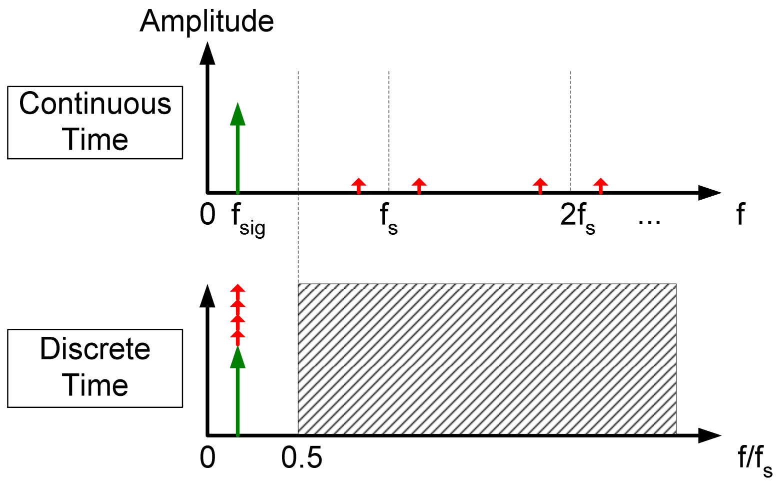


$$f_s = \frac{1}{T_s} = 1000kHz$$

$$f_{sig} = 1101kHz$$

$$v_{sig}(n) = cos\left(2\pi \cdot \frac{1101}{1000} \cdot n\right) = cos\left(2\pi \cdot \left[\frac{1101}{1000} - 1\right] \cdot n\right) = cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Consequence



- The frequencies f_{sig} and $N \cdot f_s \pm f_{sig}$ (N integer), are indistinguishable in the discrete time domain (after sampling)
- See EE102B for a rigorous mathematical treatment

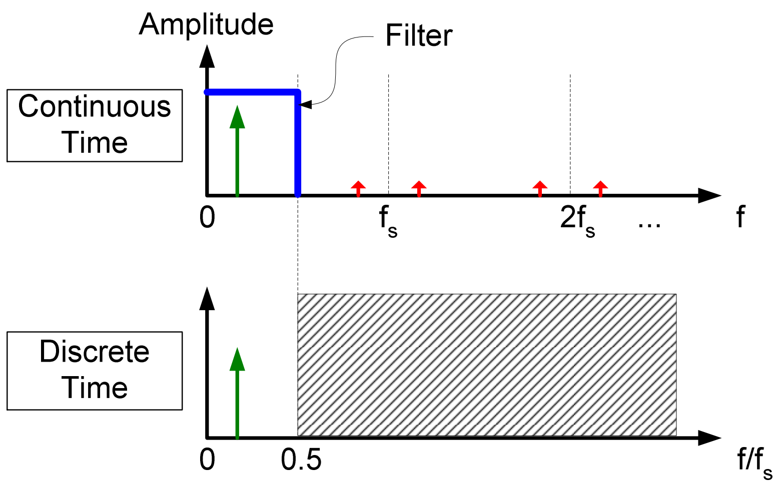
Nyquist Sampling Theorem

- In order to prevent "aliasing" we need

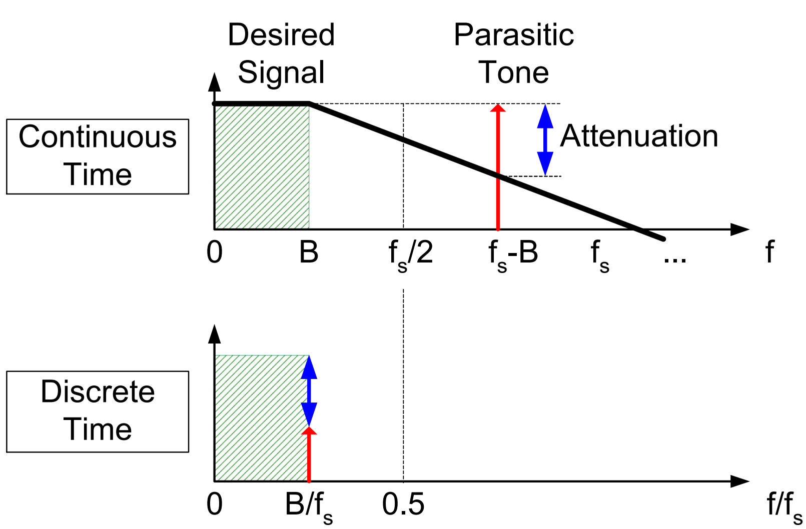
$$f_{sig,max} < \frac{f_s}{2}$$

- The sampling rate $fs=2 \cdot f_{sig,max}$ is called the Nyquist rate
- Two possibilities
  - Sample fast enough to cover all spectral components, including unwanted ones outside band of interest
  - Limit $f_{sig,max}$ through filtering → "anti-alias filter"

Brick Wall Anti-Alias Filter

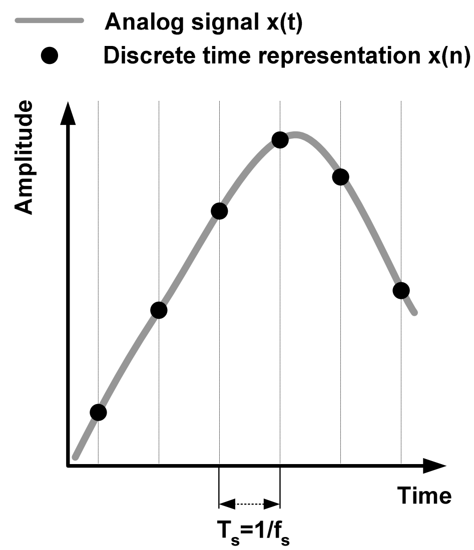


Practical Anti-Alias Filter



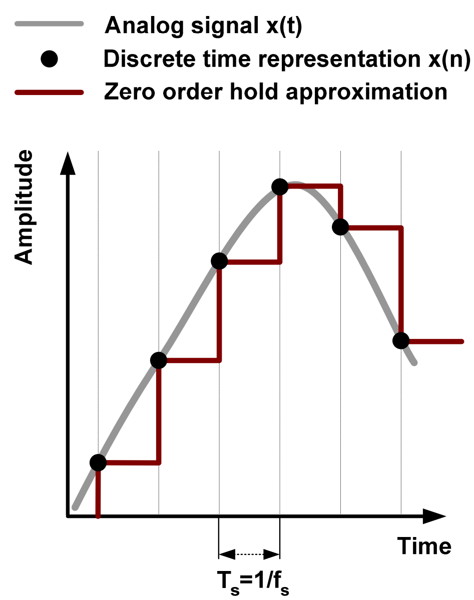
- Need to sample faster than Nyquist rate to get good attenuation
  - "Oversampling"

The Reconstruction Problem



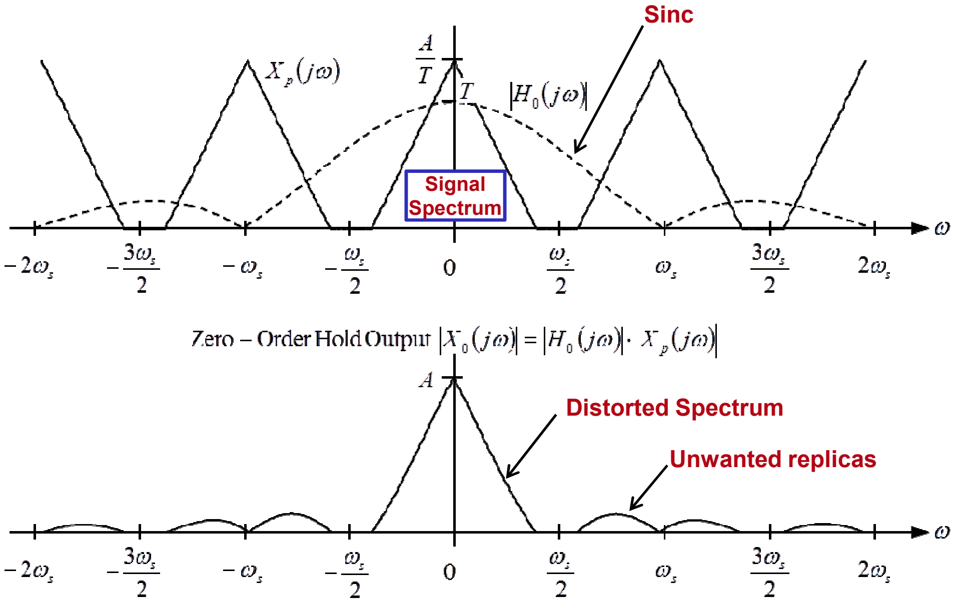
- As long as we sample fast enough, x(n) contains all information about x(t)
  - $f_s > 2 \cdot f_{sig,max}$
- How to reconstruct x(t) from x(n)?
- One can show that ideal reconstruction requires convolution with a sinc pulse
  - Not practical
  - See EE102B for the math

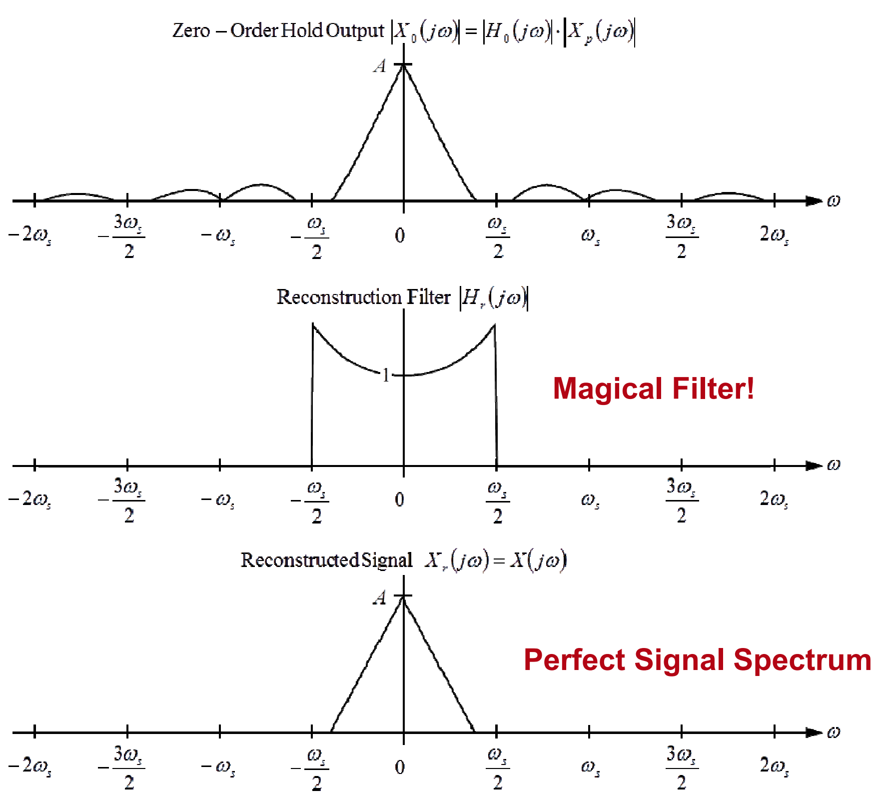
Zero-Order Hold Reconstruction



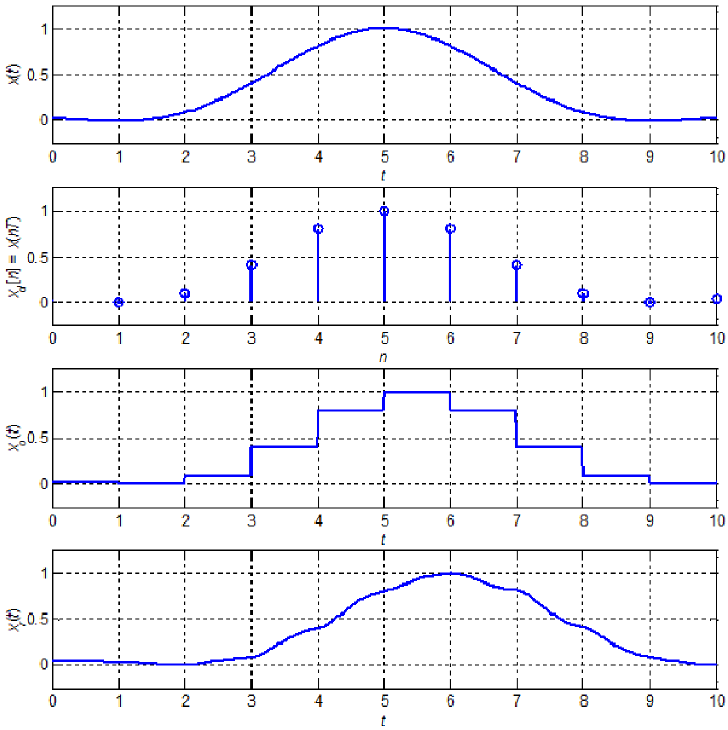
- The most practical way of reconstructing the continuous time signal is to simply "hold" the discrete time values
- It turns out that this causes sinc shaped replicas of the signal spectrum at multiples of f_s
  - Again, see EE102B for the math
- These unwanted spectral components are removed/attenuated using a reconstruction (or smoothing) filter

Example from EE102B





Time Domain Example with "Nonideal" Filter

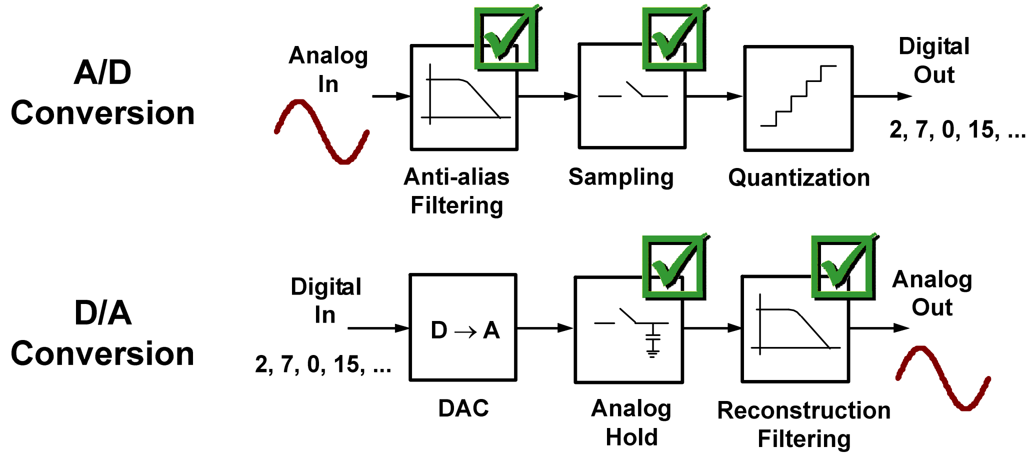


Signal after second-order Butterworth filter

How to Improve the Reconstruction

- Use a steeper filter
  - This provides stronger attenuation for the unwanted replicas
- Oversample the signal
  - This increases the spacing between the replicas and the wanted band so that the given filter will provide more attenuation
  - Furthermore, this reduces the effect of "sinc" distortion to the spectral shape (see slide 17)

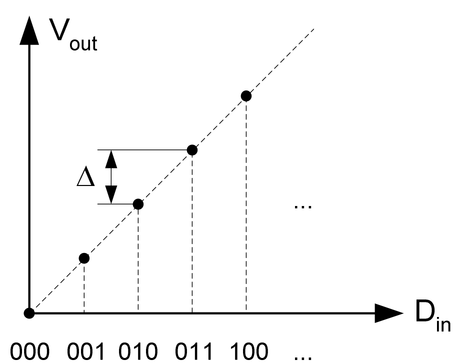
Recap



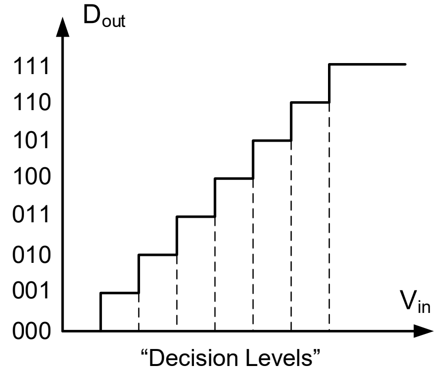
- Next, look at
  - Transfer functions of quantizer and DAC
  - Impact of quantization error

Ideal DAC Transfer Function

- Essentially a digitally controlled voltage, current or charge source
- A DAC does not introduce a quantization error

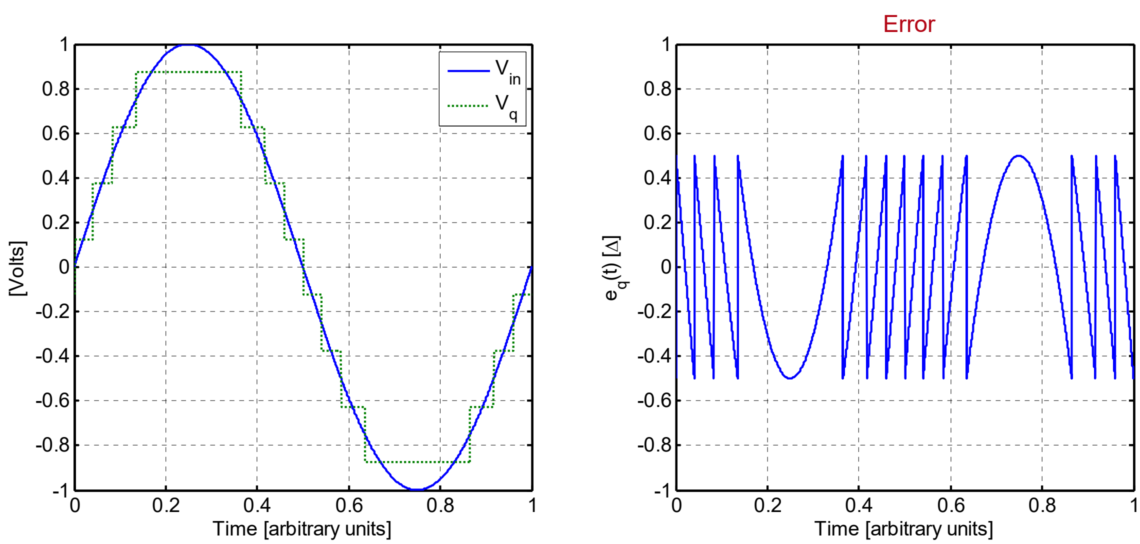


Ideal ADC Transfer Characteristic



- The inputs are mapped onto the nearest discrete output level
- Mathematically equivalent to rounding

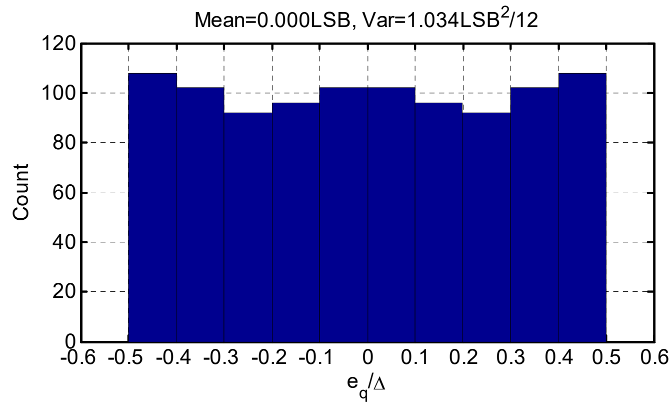
Quantizing a Sine Wave



- The introduced error is a very complicated signal that is hard to describe analytically

Quantization Error Histogram

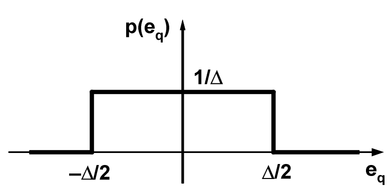
- Sinusoidal input signal with f_{sig}=101Hz, sampled at f_s=1000Hz
- 8-bit quantizer



- Distribution is "almost" uniform
- Can approximate average error power by integrating uniform distribution

Statistical Model of Quantization Error

- Assumption: $e_q(x)$ has a uniform probability density
- This approximation holds reasonably well in practice when
  - Signal spans large number of quantization steps
  - Signal is "sufficiently active"
  - Quantizer does not overload



Mean $$\overline{e_q} = \int_{-\Delta/2}^{+\Delta/2} \frac{e_q}{\Delta} de_q = 0$$

Variance $$\overline{e_q^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e_q^{\ 2}}{\Delta} de_q = \frac{\Delta^2}{12}$$

Signal-to-Quantization-Noise Ratio

- A B-bit ADC has 2^B quantization levels
- Assuming uniform e_q and a full-scale sinusoidal signal, we have

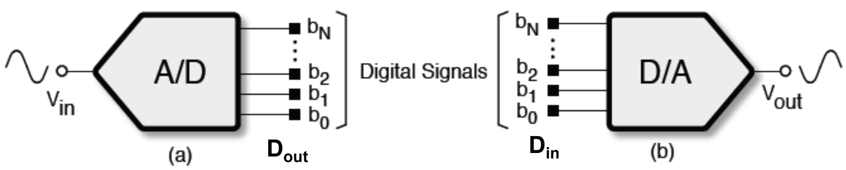
$$SQNR = \frac{P_{sig}}{P_{qnoise}} = \frac{\frac{1}{2}\left(\frac{2^B \Delta}{2}\right)^2}{\frac{\Delta^2}{12}} = 1.5 \times 2^{2B} = 6.02B + 1.76 \ \ \text{dB}$$

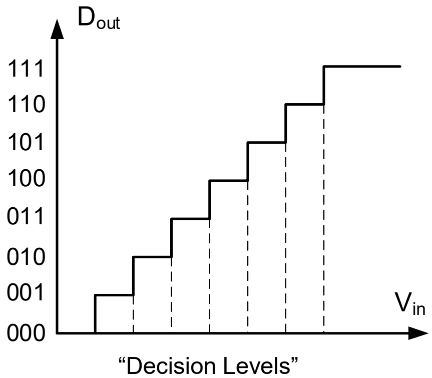
B (Number of Bits)	SQNR
8	50 dB
12	74 dB
16	98 dB
20	122 dB

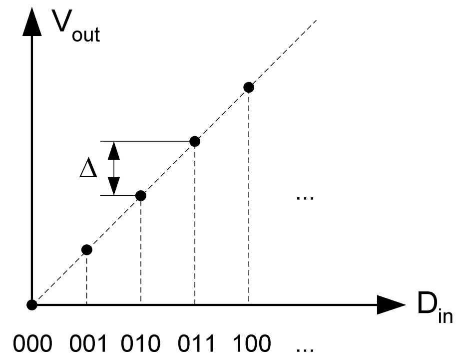
Circuit Implementation

- D/A conversion
  - Thermometer DACs
  - Binary weighted DACs
- A/D conversion
  - Flash
  - Successive approximation
  - Single slope

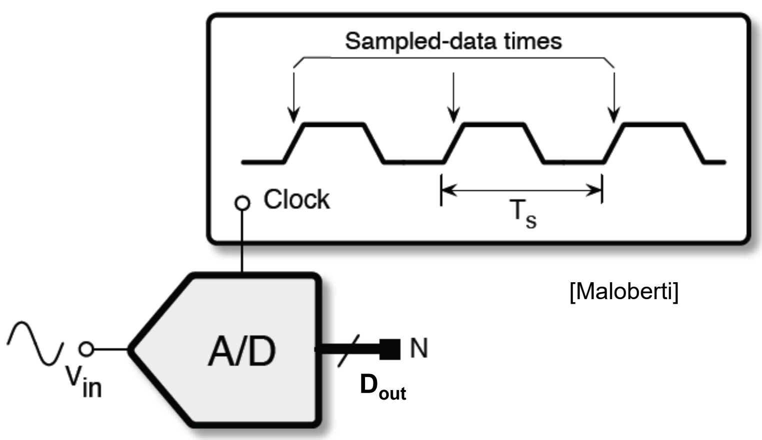
[Maloberti]







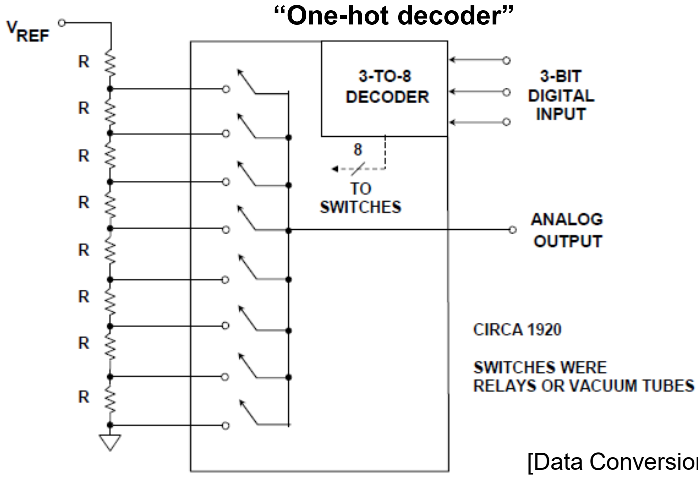
The Data Conversion is Timed by a Clock Signal



[Maloberti]

- In an ADC, the clock defines the sampling instant
- In a DAC, the clock defines the update instant of the output voltage

Resistor String DAC

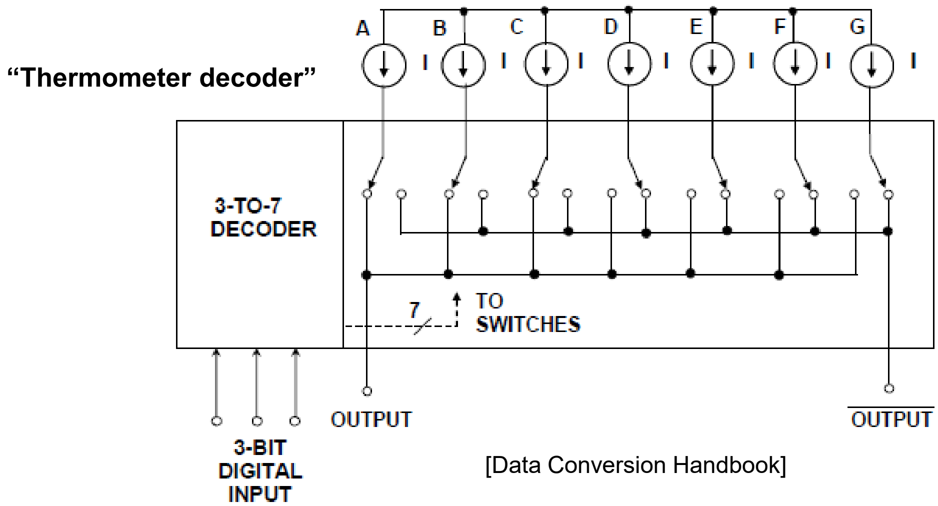


[Data Conversion Handbook]

- Switches are implemented using MOSFETs
  - Either off of operating in the triode region

Decimal	Binary	One-hot
0	000	00000001
1	001	00000010
2	010	00000100
3	011	00001000
4	100	00010000
5	101	00100000
6	110	01000000
7	111	10000000

Similar Idea Using Currents – Thermometer Current Steering DAC

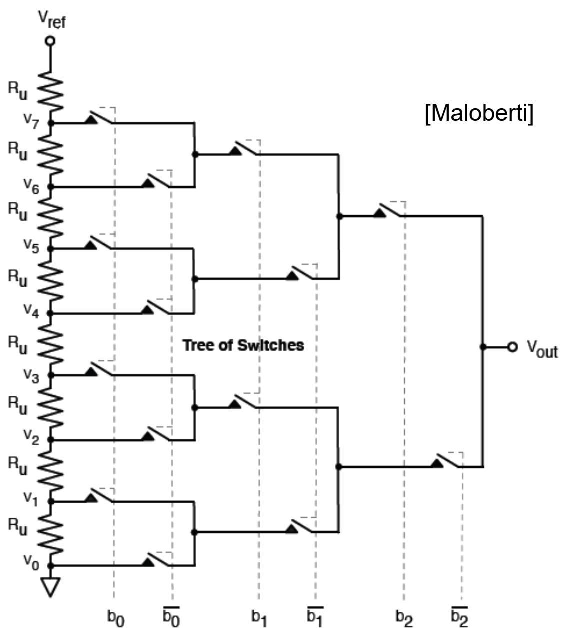


[Data Conversion Handbook]

- For a "single ended" output, $\overline{\text{OUTPUT}}$ can be grounded
- The output can be fed to a resistor or the virtual ground of an opamp

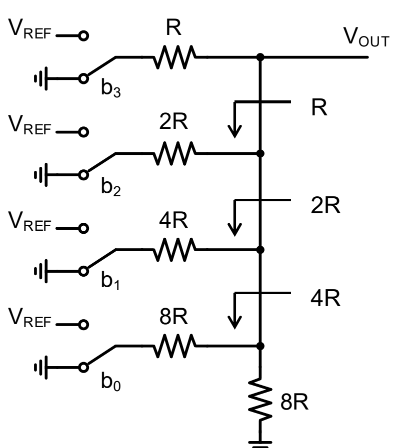
Decimal	Binary	Thermometer
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

Eliminating the Encoder



No encoder, but lots of switches

Binary Weighted Resistor DAC

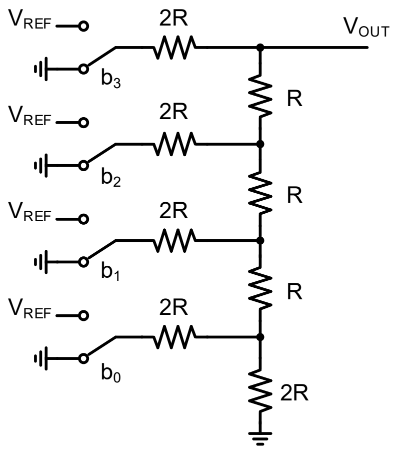


$b_0 \ldots b_3 \in \{0,1\}$

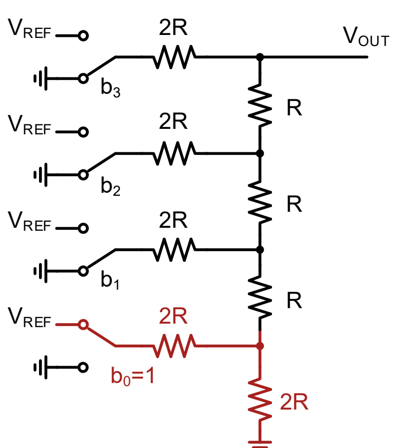
$$V_{OUT} = \frac{V_{REF}}{2}\left(\frac{b_3}{1} + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8}\right)$$

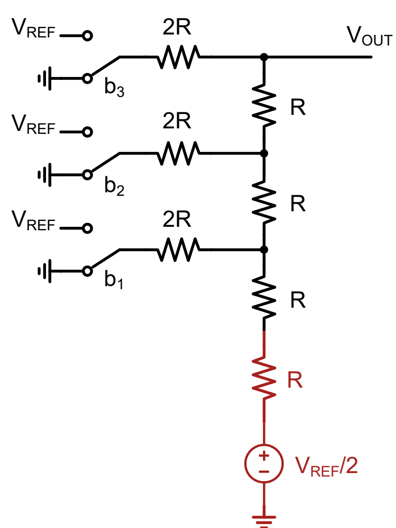
- No encoder, but component spread becomes large for high resolution
  - Think about a 16-bit version of the above circuit

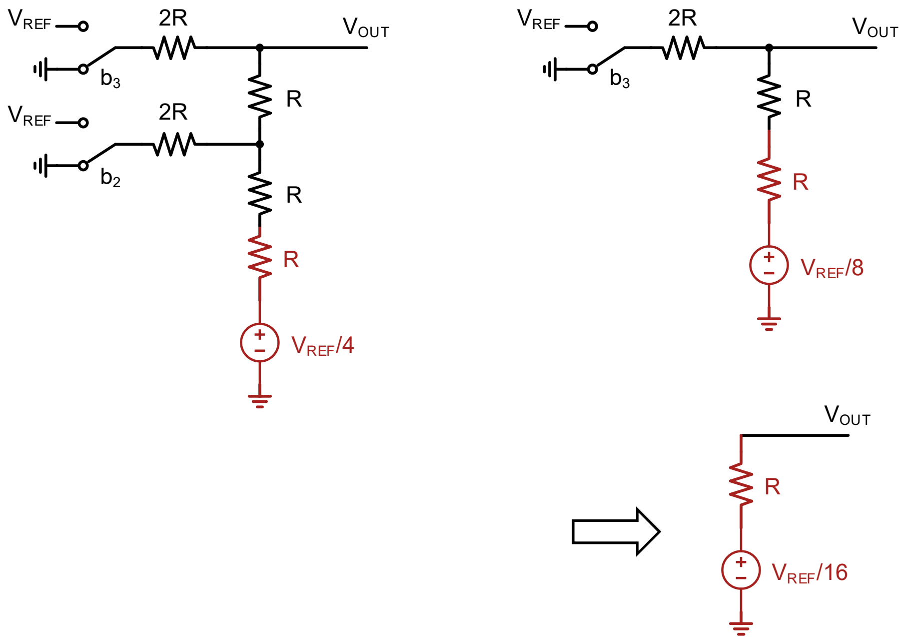
R-2R DAC



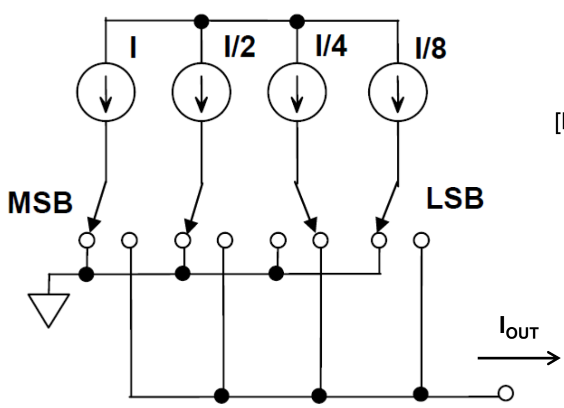
- Analyze using successive application of Thevenin
- Let's look at the LSB as an example







Binary Weighted Current Steering DAC



[Data Conversion Handbook]

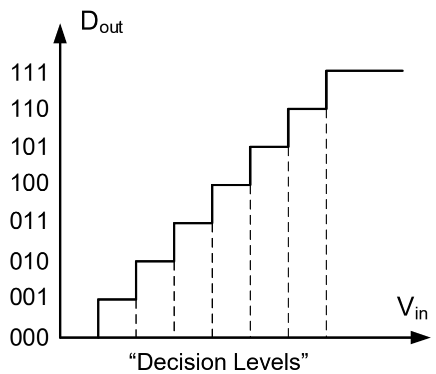
- Similar to binary weighted resistor DAC
- There is no current steering equivalent for the R-2R architecture

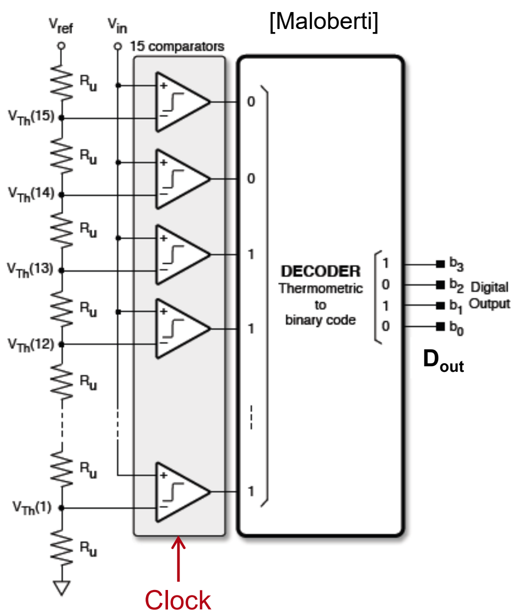
Summary on DACs

- DACs can be built in lots of different ways; we just looked at a few
- Architectural choices are often driven by the need to limit complexity or component spread

- What we haven't covered
  - Switched capacitor DACs
  - Opamp-based circuits
  - Segmentation (combining binary and thermometer sections)
  - Nonidealities
  - …

Flash ADC

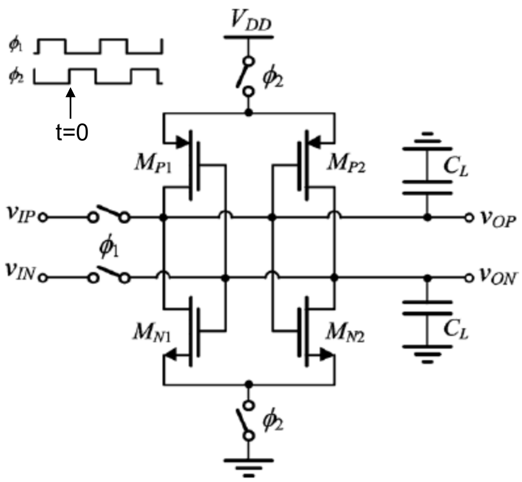




Ideal voltage comparator: $V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$

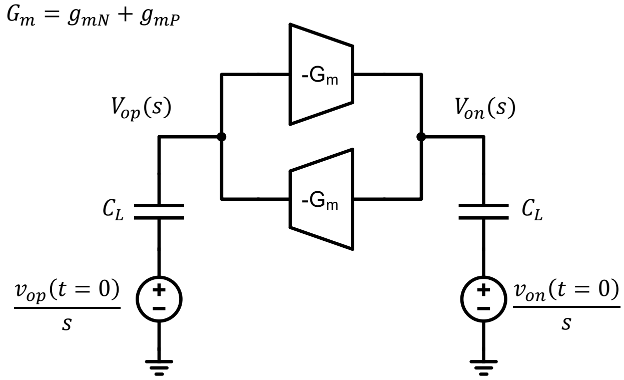
- Decision levels are generated by a resistor ladder and a bank of voltage comparators compares the input against these levels

Basic Latch-Based Voltage Comparator



Circuit model during ϕ_2

$G_m = g_{mN} + g_{mP}$



ϕ1: Set up initial conditions
ϕ2: Enable positive feedback

$$0 = sC_L\left(V_{op}(s) - \frac{v_{op}(t=0)}{s}\right) + G_m V_{on}(s)$$

$$0 = sC_L\left(V_{on}(s) - \frac{v_{on}(t=0)}{s}\right) + G_m V_{op}(s)$$

$$0 = sC_L\left(V_{op}(s) - \frac{v_{op}(t=0)}{s}\right) + G_m V_{on}(s)$$

$$0 = sC_L\left(V_{on}(s) - \frac{v_{on}(t=0)}{s}\right) + G_m V_{op}(s)$$

$$V_{on}(s) = -\frac{sC_L}{G_m}\left(V_{op}(s) - \frac{v_{op}(t=0)}{s}\right)$$

$$V_{op}(s) = -\frac{sC_L}{G_m}\left(V_{on}(s) - \frac{v_{on}(t=0)}{s}\right)$$

Define:

$$V_{od}(s) = V_{op}(s) - V_{on}(s)$$

$$\tau = \frac{C_L}{G_m}$$

$$V_{od}(s) = s\tau V_{od}(s) + \tau v_{od}(t=0)$$

$$V_{od}(s) = v_{od}(t=0)\frac{\tau}{1 - s\tau}$$

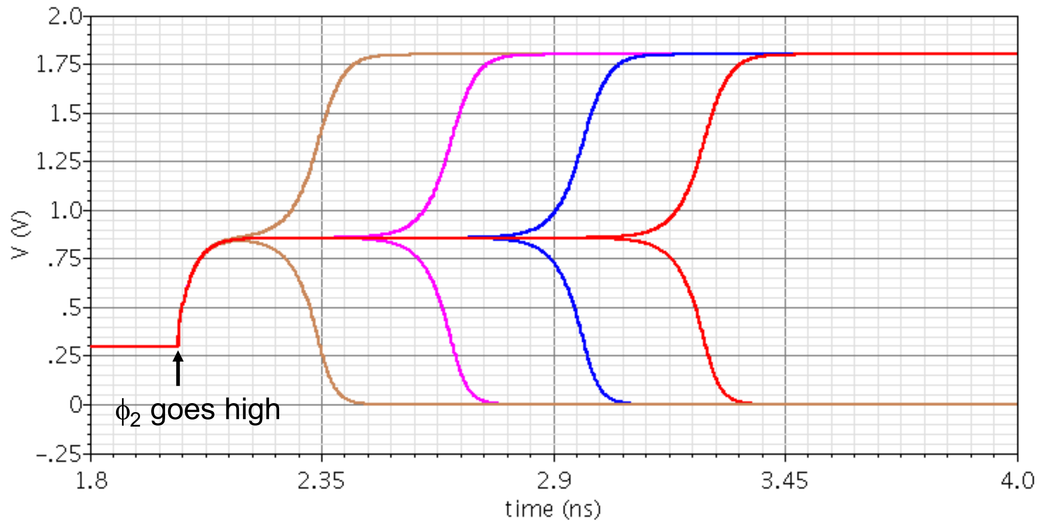
RHP Pole

$$\boxed{v_{od}(t) = v_{od}(t=0)e^{t/\tau}}$$

The differential output grows exponentially, with the sign of the initial condition

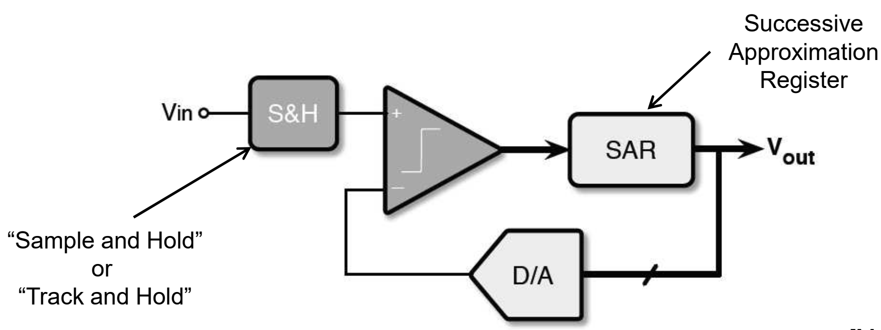
Typical Waveforms

Nodes v_{OP} and v_{ON} for initial v_{OD} of 1mV, 1μV, 1nV and 1pV

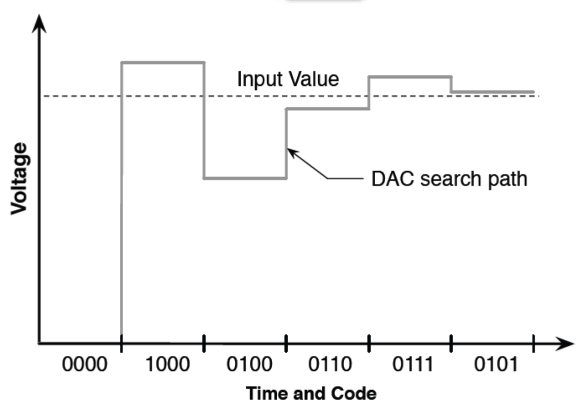


- This is the fastest possible way to detect the polarity of a signal

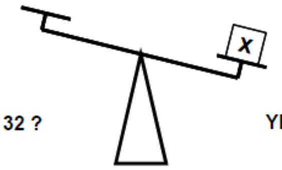
SAR ADC



[Maloberti]



Alternative View



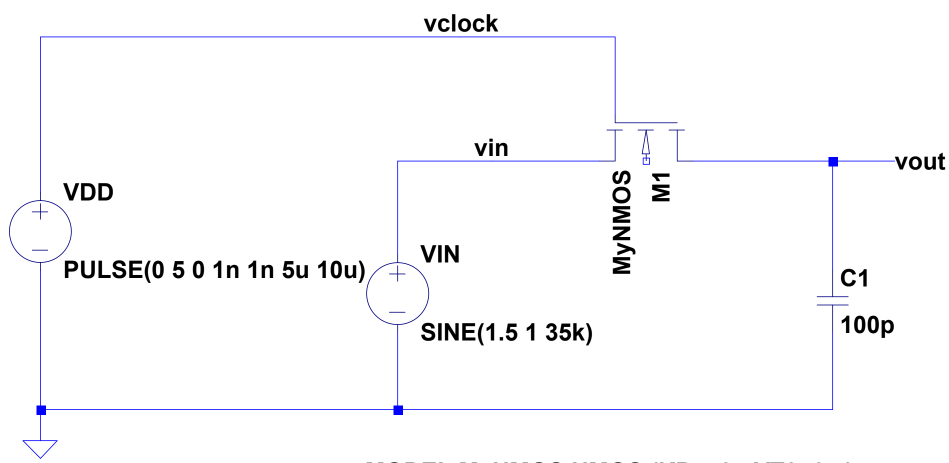
ASSUME X = 45

TEST		
IS X ≥ 32 ?	YES → RETAIN 32 →	1
IS X ≥ (32 +16) ?	NO → REJECT 16 →	0
IS X ≥ (32 +8) ?	YES → RETAIN 8 →	1
IS X ≥ (32 +8 + 4) ?	YES → RETAIN 4 →	1
IS X ≥ (32 +8 + 4 + 2) ?	NO → REJECT 2 →	0
IS X ≥ (32 +8 + 4 + 2 + 1) ?	YES → RETAIN 1 →	1

TOTALS: $X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2$

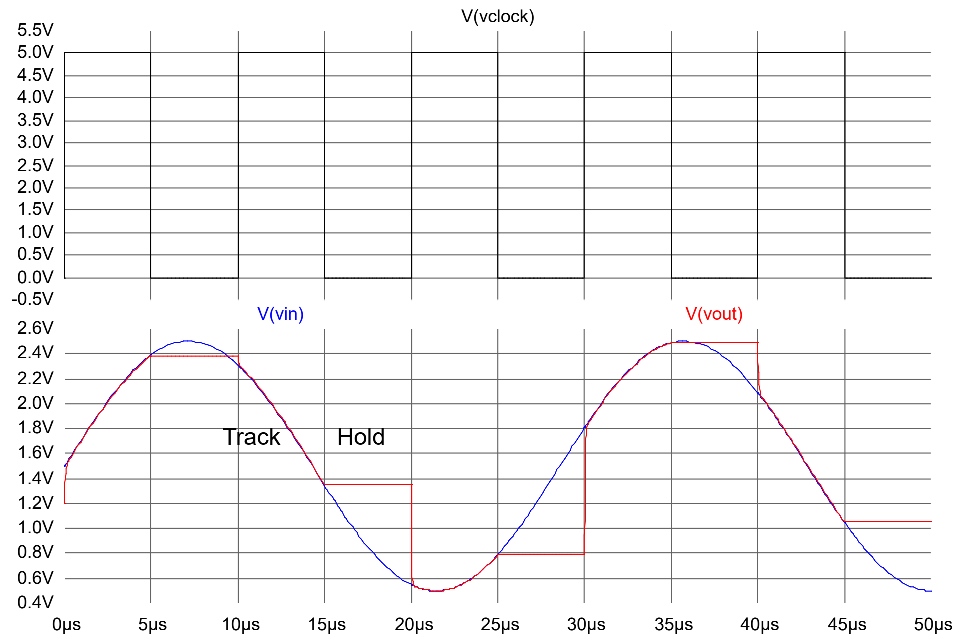
[Data Conversion Handbook]

Basic Track and Hold Circuit



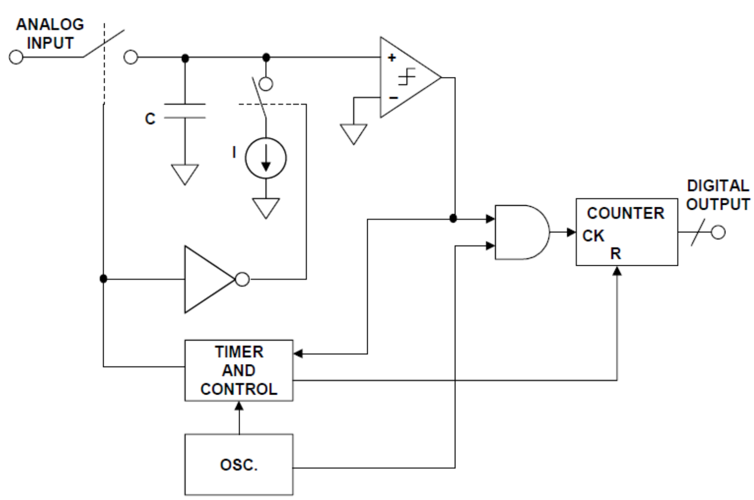
.MODEL MyNMOS NMOS (KP=50u VT0=0.5)
.tran 50u

Waveforms



Single-Slope ADC

- Many different implementations exist; below is the simplest variant
- Main idea is to count the number of clock cycles it takes to discharge the sampled signal with a current source



Comparison

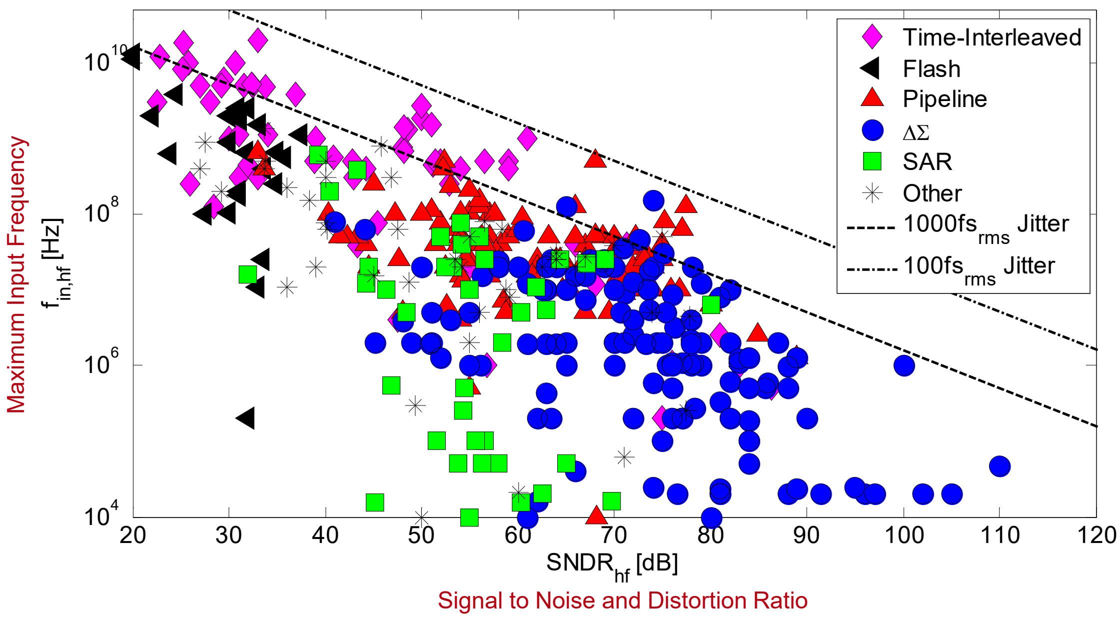
	Clock Cycles Per Conversion	Complexity
Flash	~1	High ~2^B
SAR	~B	Medium
Single Slope	~2^B	Low (no DAC)

B = number of bits

Summary on ADCs

- ADCs can be built in lots of different ways; we just looked at a few
- The choice of architecture is often driven by a reasonable tradeoff between complexity and speed
- What we haven't covered
  - Oversampling ADCs (Delta-sigma ADCs)
  - Pipeline ADCs
  - Time interleaving
  - Nonidealities
  - …

Performance of State-of-the-Art ADCs



B. Murmann, "ADC Performance Survey 1997-2014," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

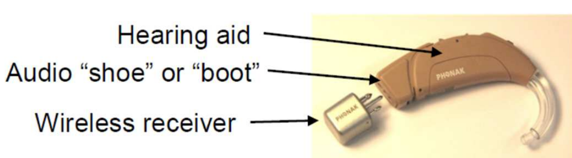
Chapter 20

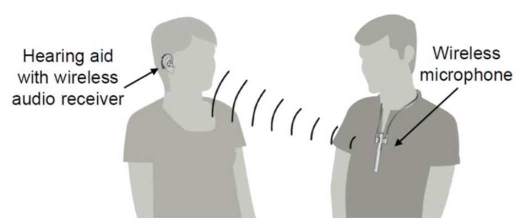
Summary

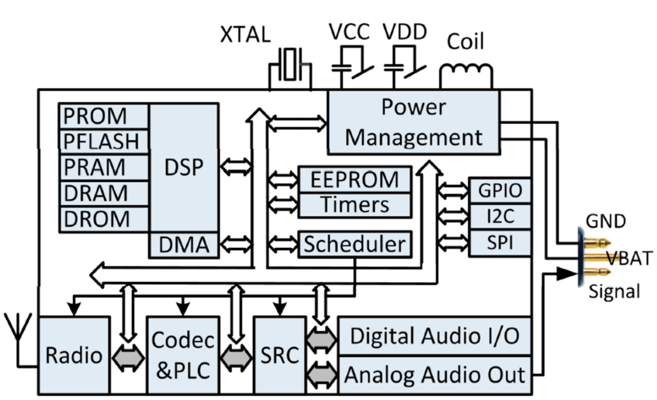
Boris Murmann

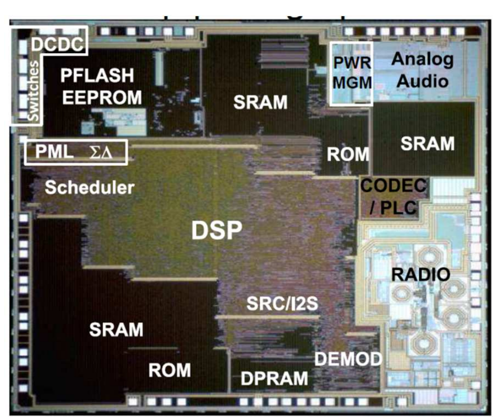
Stanford University

Modern Circuits Are Complex



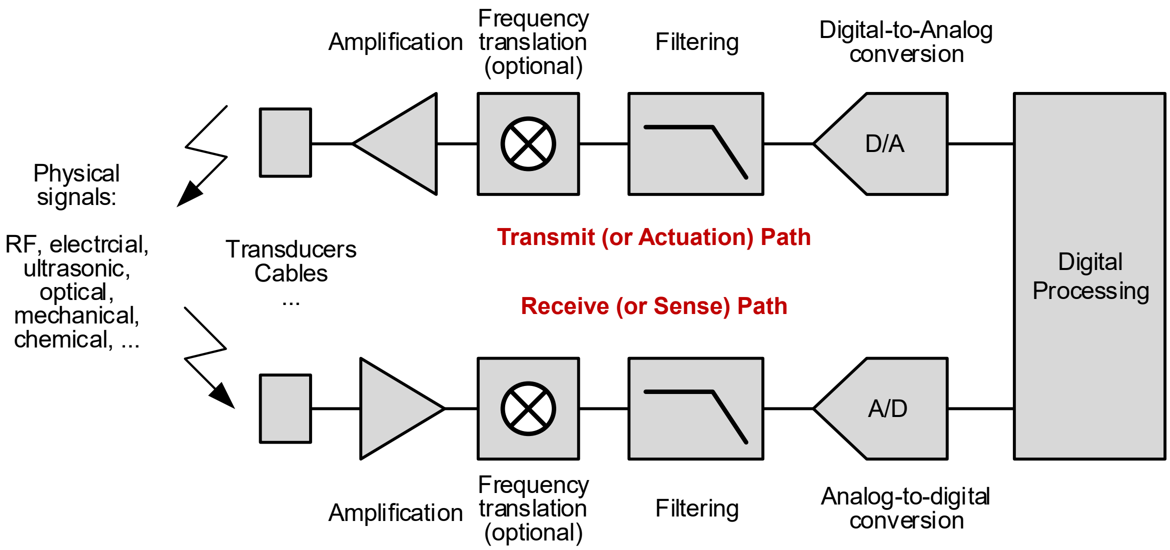






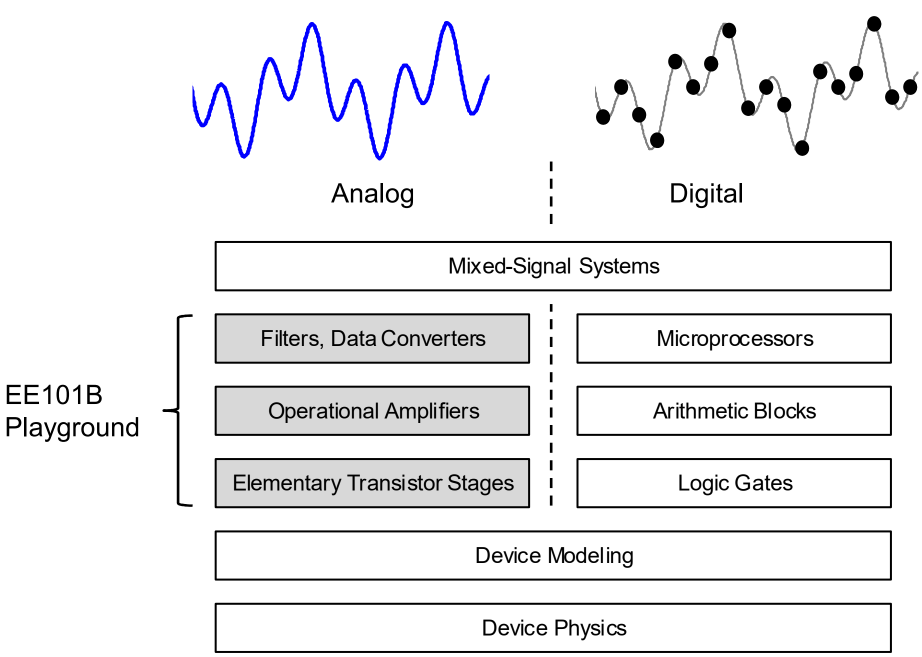
[El-Hoiydi, 2014 International Solid-State Circuits Conference (ISSCC)]

Managing Complexity: Block Abstraction



- Almost any meaningful electronic mixed-signal system can be represented by this generic block diagram

Managing Complexity: Hierarchical Abstraction



Topics Covered in This Course

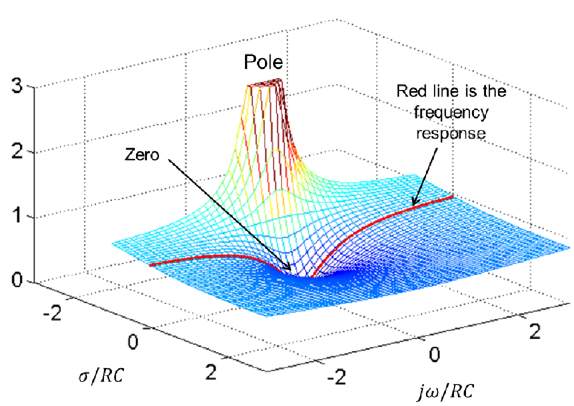
- Modeling and analysis of analog gain stages
  - MOSFET operation
  - Biasing
  - Small-signal analysis
  - Two-port models
- Laplace transform for circuit designers
  - Frequency response
  - Step response
- Opamp-based feedback circuits
  - Basic analysis
  - Stability and frequency compensation
  - Oscillators
  - Analog filters
- Circuit simulation
- A/D and D/A conversion

Main Objective: Build up a Solid Toolkit

- MOSFET modeling
  - MOSFET physics are very complicated
  - Used the simplest possible model to minimize complexity while retaining most important effects
- Small-signal approximation
  - Electronic circuits are not perfectly linear, but using a linear model greatly simplifies their analysis
  - Use large-signal equations to find bias point
  - Linearize all components at the operating point
  - Continue analysis with linear small-signal model
    - Can use linear tricks, like superposition
    - Apply known results as much as possible; do not blindly grind through KCL/KVL!
- Two-port modeling
  - Creates an additional level of abstraction
  - Lets us think about cascading multiple stages

- Energy storage elements
  - Basic intuition
    - C is an open at DC, short at high frequencies
    - L is a short at DC, open at high frequencies
  - Nodal equations become differential equations with L and/or C present
    - But writing/solving differential equations for circuit analysis is tedious and cumbersome
- LTI system analysis, Fourier transform, H(jω)
  - A step in the right direction
  - Recognize that system is fully described by impulse response; convolution with impulse response gives output
  - Convolution in the time domain → Multiplication in the frequency domain
  - Eigenfunction $e^{j\omega t}$

- Laplace transform, H(s)
  - "The" analysis tool for electrical engineers
  - Eigenfunction e^{st}
  - Lets us describe arbitrary linear systems, even unstable ones (e.g. oscillators during start-up)
  - System is fully described by the location of poles and zeros in the s-plane



- Laplace transform of components
  - $Z_C = 1/sC$, $Z_L = sL$
  - Model initial conditions using independent sources in series or parallel
- Using Laplace to find the step response
  - Set input to 1/s, multiply with H(s), use inverse Laplace transform to find time domain output
  - Often requires partial fraction expansion
- Using Laplace to find the frequency response
  - Set $s = j\omega$ → Fourier transform
  - Evaluate magnitude and phase, create a Bode plot
  - Understand asymptotes in Bode plot
    - What happens at low/high frequencies when certain components become open/short
  - Understand impact of real LHP/RHP zeros and LHP poles on phase and magnitude

- Second order systems
  - The "bread and butter" system model; applicable to many different circuits
  - Q factor is a proxy that tells us whether the system rings (time domain) or peaks (frequency domain)
- Filter design
  - Place poles and zeros "strategically" in the s-plane to meet certain objectives, e.g.
    - Maximally flat response (Butterworth)
    - Steepest possible roll-off (Elliptic)
    - Maximally flat group delay (Bessel)
      - Desired when wave-shape of time domain signal is important
  - Unfortunately it is impossible to get a sharp roll-off and well-behaved step response; one must pick a trade-off

- Basic op-amp circuit analysis
  - Find ideal closed-loop transfer function by assuming ideal opamp model (infinite gain, virtual ground)
  - Then find loop gain (T) to quantify deviation from ideality

$$A_{CL} = A_{CL,ideal} \frac{T}{1+T}$$

- Frequency response of opamp circuits
  - Single-pole opamp
    - Closed-loop BW is equal to unity gain frequency of T(jω) → $f_{3dB} = f_{u1}$
  - Two-pole opamp
    - Closed-loop BW is still approximately equal to f_{u1}, but exact value depends on position of second pole (which must occur beyond f_{u1})
  - More than two poles → approximate with two pole model

- Stability of feedback circuits
  - Most general criterion is BIBO (somewhat useless)
  - For a loop consisting of stable LTI systems, we can apply the Bode criterion
    - Phase margin, gain margin
  - First order system has 90º phase margin (boring)
  - Second order system has a one-to-one mapping of phase margin and Q of closed loop poles
- Frequency compensation
  - Tweak a feedback circuit to adjust/improve its phase margin
  - Most off the shelf opamps are already properly compensated
    - Dominant pole plus other poles beyond f_{u1}

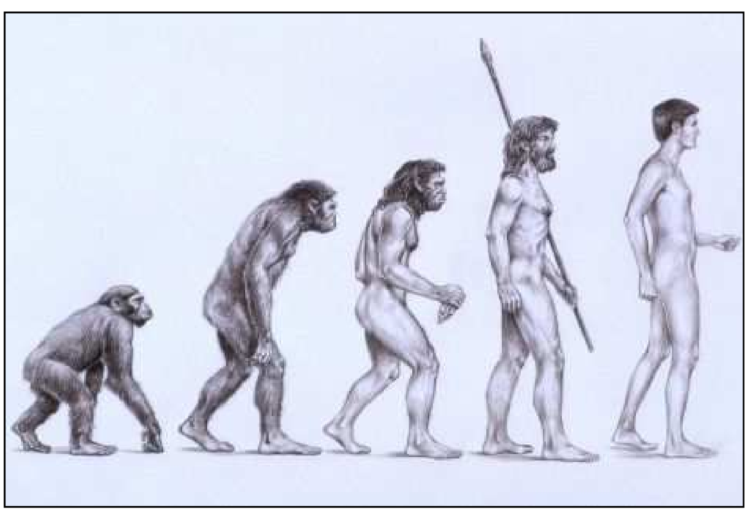
- Oscillators
  - What bothers us in amplifiers is great for building oscillators
  - Barkhausen criterion
  - Roughly speaking, poles are initially in the right half plane, then snap onto the jω axis → steady-state oscillations
  - Covered phase shift, Wien, LC and xtal oscillators
- Data converters
  - ADC: Sampling and quantization
  - DAC: Zero-order hold reconstruction
  - Both typically require filters
    - Anti-aliasing and image rejection
  - Many different architectures exist to meet different points objectives in the speed/complexity trade-off space

- Circuit simulation
  - Circuit simulator is nothing but a powerful numerical solver
  - OP, DC, AC, TRAN analysis are very similar to the way we look at/analyze circuits by hand
  - Garbage in → garbage out
- The coolest hand analysis tools ever
  - OCTC analysis
    - Provides a first order (conservative) BW estimate using divide and conquer
    - Must know potential pitfalls
  - Blackman's impedance formula
    - Quickly compute the input/output impedances of a feedback circuit

Where to Go From Here?

	Autumn	Winter	Spring	
Sophomore		EE 101A Circuits I	EE 101B Circuits II	
Junior Senior Co-term	EE 114 Analog IC I	EE 214B Analog IC II		Integrated (IC) Analog
	EE 122A Analog Lab	EE 133 Analog Comm. Lab		Board-Level Analog
	EE 124 Neuro-Bio	EE 122B Bio-Instruments		Neuro-Bio Electronics
	EE 153 Power Electronics	EE 254 Adv. Power Electr.		Power Electronics
	EE 118 Mechatronics	Eng. 105 Feedback Controls		Mechatronics
	EE 271 Digital IC	EE 313 Digital Memory		Digital Circuits

The Evolution of a Circuit Designer…



EE101A,B	EE114/214A	EE214B	EE313
	EE122A/B	EE271	EE314A,B
	EE133	EE254	EE315
	EE153		