STANFORD UNIVERSITY
Department of Electrical Engineering

EE214B: Advanced Analog Integrated Circuit Design

https://canvas.stanford.edu/courses/74180

TIME:	Class: MWF 10:30-11:20 AM, Gates B03 Review Session: Friday, 12:30-1:20, Huang18
INSTRUCTOR: Email: Office hours:	Boris Murmann murmann@stanford.edu See course website.
TAs Email: Office hours:	Vlad Kesler ee214b-tas@mailman.stanford.edu See course website.
ADMIN: Email: Phone: Office:	Ann Guerra guerra@par.stanford.edu (650) 725-3725 Allen-207

GRADING:

Homework	20% (lowest score will be dropped)
Midterm Exam	30%
Project	20%
Final Exam	30%

COURSE READER:	B. Murmann, EE214B – Advanced Analog Integrated Circuit Design Hardcopies available at Stanford Bookstore, Softcopies available online
REFERENCE TEXTS:	Jespers and Murmann, Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables, Cambridge, 2017 (Link)
	Tony Chan Carusone, David A. Johns and Kenneth W. Martin, Analog Integrated Circuit Design, 2nd Edition, Wiley, 2011 (Link)
	Gray, Hurst, Lewis and Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009 (Link)
GROUP DISCUSSIONS:	Please use the "Discussions" feature on Canvas for group discussions or to post questions.
COURSE DESCRIPTION:	Analysis and design of analog integrated circuits in advanced MOS and bipolar technologies. Device operation and compact modeling in support of circuit simulations needed for design. Emphasis on quantitative evaluations of performance using hand calculations and circuit simulations; intuitive approaches to design. Analytical treatment of noise; analysis and design of feedback circuits. Design of archetypal analog blocks such as high-speed gain stages and transimpedance amplifiers. Prerequisite: EE114/EE214A or equivalent.

Course Calendar (Tentative)

Date	Lecture	Assignments
Mon 01/08	1: Introduction	
Wed 01/10	2: MOSFET Modeling	HW1 out
Fri 01/12	3: MOSFET Modeling	
Mon 01/15	**NO CLASS (Martin Luther King Day)**	
Wed 01/17	4: g_m/I_D-Based Design	HW1 due, HW2 out
Fri 01/19	5: g_m/I_D-Based Design	
Mon 01/22	6: Electronic Noise	
Wed 01/24	7: Electronic Noise	HW2 due, HW3 out
Fri 01/26	8: Electronic Noise	
Mon 01/29	9: Electronic Noise	
Wed 01/31	10: Mismatch	HW3 due, HW4 out
Fri 02/02	11: OTA Design Preliminaries	
Mon 02/05	12: OTA Design Preliminaries	
Wed 02/07	13: OTA Design Preliminaries	HW4 due, HW5 out
Thu 02/08	14: OTA Design Preliminaries (Thornton 102, 10:30-11:20)	
Fri 02/09	15: Load-Compensated OTAs	
Mon 02/12	**NO CLASS**	
Mon 02/12	**MIDTERM EXAM (6:30-8:00 PM, Room 370-370)**	
Wed 02/14	**NO CLASS**	
Thu 02/15	16: Load-Compensated OTAs (Thornton 102, 10:30-11:20)	
Fri 02/16	17: Two-Stage OTAs	HW5 due, Project out
Mon 02/19	**NO CLASS (Presidents' Day)**	
Wed 02/21	18: Two-Stage OTAs	
Fri 02/23	19: Bipolar Junction Transistors	
Mon 02/26	20: Bipolar Junction Transistors	Project I due
Wed 02/28	21: Bipolar Junction Transistors	
Fri 03/02	22: Elementary BJT Circuits	
Mon 03/05	23: Feedback TIA design	
Wed 03/07	24: Feedback TIA design	
Fri 03/09	25: Distortion analysis	Project II due, HW6 out
Mon 03/12	26: Distortion analysis	
Wed 03/14	27: Distortion analysis, Final preparation	
Fri 03/16	**PROJECT PRESENTATIONS (Gates B03, 10:00-11:20)**	HW6 due
Thu 03/22	**FINAL EXAM (Gates B03, 8:30-10:00 AM)**	

FAQ

Q: How should I submit my homework?
A: We will use electronic submission through Canvas. Do not email your homework to the teaching staff.

Q: What is the late submission policy?
A: All assignments are due on the specified date and time, sharp. This is enforced by the electronic submission system.

Q: Which program will we use for circuit simulation?
A: The primary simulator for this course is HSpice. You can access this tool via your instructional computer account. Please refer to the "CAD Basics" handout on the course web site for further information.

Q: Can I use a different circuit simulator?
A: You may use other Spice variants at your "own risk."

Q: I am a remote student, how can I access and run HSpice?
A: You can log into your instructional account via SSH and VNC (see "CAD Basics" handout). You may also refer to: https://itservices.stanford.edu/service/sharedcomputing/loggingin

Q: I am a remote student; how can I access online libraries such as IEEE Xplore?
A: You can use EZproxy to log into access-restricted sites, for example:
http://ezproxy.stanford.edu/login?url=http://ieeexplore.ieee.org

Q: I cannot attend your scheduled office hours. Are you available at other times?
A: Feel free to email the instructor to set up a meeting on an as-needed basis.
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Q: I am an SCPD student, and I must get a grade of B or higher, otherwise I have to pay. Can you guarantee that I won't have to pay?
A: No, of course not. You earn your grade; we don't arbitrarily assign it. To minimize the likelihood of having to pay, stay current on the homework and, especially, allot plenty of time to do a good job on the design project. Many SCPD students find themselves in trouble time-wise, because of customer visits, unexpected tape-out problems, etc., at their place of employment. Our advice is to expect the unexpected, and budget enough extra time for EE214B.

Q: I need to take the midterm/final exam at other than the scheduled time. May I?
A: Such arrangements are made on a case-by-case basis, and we cannot guarantee flexibility in this matter. The most common acceptable reason is a demonstrable scheduling conflict with another course (which would imply that you are taking two courses that are scheduled at the same time). As an example, "Being able to catch a cheaper flight for a vacation" is not a suitable reason. Please alert us as soon as possible.