STANFORD UNIVERSITY
Department of Electrical Engineering

EE214B: Advanced Integrated Circuit Design

https://canvas.stanford.edu/courses/92946

TIME:	Class: MWF 10:30-11:20 AM, Gates B03 Review Sessions: Fri 2/15 (midterm preparation, 12:30-1:20, Gates B03), Thurs 3/14 (final preparation, 1:30-2:20, Gates B01)
INSTRUCTOR:	Boris Murmann
Email:	murmann@stanford.edu
Office hours:	See course website.
TAs	Vlad Kesler
Email:	ee214b-tas@mailman.stanford.edu
Office hours:	See course website.
ADMIN:	Ann Guerra
Email:	guerra@par.stanford.edu
Phone:	(650) 725-3725
Office:	Allen-207

GRADING:		
	Homework	30% (lowest two scores will be dropped)
	Midterm Exam	30%
	Final Exam	40%

REFERENCE TEXTS:

Jespers and Murmann, Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables, Cambridge, 2017 (Link)

Chan Carusone, Johns and Martin, Analog Integrated Circuit Design, 2nd edition, Wiley, 2011 (Link)

Gray, Hurst, Lewis and Meyer, Analysis and Design of Analog Integrated Circuits, 5th edition, Wiley, 2009 (Link)

Hodges, Jackson, and Saleh, Analysis and Design of Digital Integrated Circuits, 3rd edition, McGraw Hill, 2004 (Link)

GROUP DISCUSSIONS:

Piazza signup: http://piazza.com/stanford/winter2019/ee214b

COURSE DESCRIPTION:

Analysis and design of analog and digital integrated circuits in advanced CMOS technology. Emphasis on compact modeling of performance limiting aspects and intuitive approaches to design. Analytical treatment of noise; analog circuit sizing using the transconductance to current ratio; analysis and design of feedback circuits. Delay analysis of digital logic gates; decoder design using logical effort. CMOS image sensor design is used as a motivating example.

Prerequisite: EE114/EE214A or equivalent. Recommended: EE271.

Course Calendar (Tentative)

Date	Lecture	Assignments
Mon 01/07	1: Introduction	
Wed 01/09	2: Image sensor basics	HW1 out
Fri 01/11	3: Shot noise, SNR and DR	
Mon 01/14	4: Fixed-pattern noise, mismatch	
Wed 01/16	5: Thermal noise	HW1 due, HW2 out
Fri 01/18	6: MOSFET thermal and flicker noise	
Mon 01/21	**NO CLASS (Martin Luther King Day)**	
Wed 01/23	7: Noise analysis in circuits	HW2 due, HW3 out
Fri 01/25	8: Noise analysis in circuits	
Mon 01/28	9: Feedback Circuit Analysis using Behavioral OTA Models	
Wed 01/30	10: Feedback Circuit Analysis using Behavioral OTA Models	HW3 due, HW4 out
Fri 02/01	11: Feedback Circuit Analysis using Behavioral OTA Models	
Mon 02/04	12: Modeling of advanced MOSFETs	
Wed 02/06	13: Modeling of advanced MOSFETs	HW4 due, HW5 out
Fri 02/08	14: g_m/I_D-based design	
Mon 02/11	15: Fully differential OTAs	
Wed 02/13	16: Fully differential OTAs	HW5 due
Fri 02/15	17: Fully differential OTAs	
Mon 02/18	**NO CLASS (Presidents' Day)**	
Wed 02/20	**NO CLASS (ISSCC)**	HW6 out
Wed 02/20	**MIDTERM EXAM (6:30-8:00 PM, Thornton 102)**	
Fri 02/22	18: Interconnect and Elmore delay	
Mon 02/25	19: CMOS logic gates	
Wed 02/27	20: Optimal gate sizing	HW6 due, HW7 out
Fri 03/01	21: Logical effort	
Mon 03/04	22: Decoder design	
Wed 03/06	23: Gate delay modeling revisited	HW7 due, HW8 out
Fri 03/08	24: Low-power digital design	
Mon 03/11	25: Chip I/O	
Wed 03/13	26: Research example	HW8 due
Fri 03/15	27: Class summary	
Thu 03/21	**FINAL EXAM (8:30-11:30 AM, Gates B03)**	

FAQ

Q: How should I submit my homework?
A: You will submit your work online. Do not email your homework to the teaching staff.

Q: What is the late submission policy?
A: All assignments are due on the specified date and time, sharp. This is enforced by the online submission system.

Q: Which program will we use for circuit simulation?
A: The primary simulator for this course is HSpice. You can access this tool via your instructional computer account. Please refer to the "CAD Setup" document on Canvas.

Q: Can I use a different circuit simulator?
A: You may use other Spice variants at your "own risk" (i.e., we will not provide any support or help with debugging and checking the results).

Q: I am a remote student, how can I access and run HSpice?
A: You can log into your instructional account using the tools described in the "CAD Setup" document available on Canvas.

Q: I am a remote student; how can I access online libraries such as IEEE Xplore?
A: You can use EZproxy access to electronic library resources, as described here. We recommend the EZproxy “bookmarklet” option.

Q: I cannot attend your scheduled office hours. Are you available at other times?
A: Feel free to email the instructor to set up a meeting on an as-needed basis.
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Q: I am an SCPD student, and I must get a grade of B or higher, otherwise I have to pay. Can you guarantee that I won’t have to pay?
A: No, of course not. You earn your grade; we don’t arbitrarily assign it. To minimize the likelihood of having to pay, stay current on the homework and, especially, allot plenty of time to do a good job on the design project. Many SCPD students find themselves in trouble time-wise, because of customer visits, unexpected tape-out problems, etc., at their place of employment. Our advice is to expect the unexpected, and budget enough extra time for EE214B.

Q: I need to take the midterm/final exam at other than the scheduled time. May I?
A: Such arrangements are made on a case-by-case basis, and we cannot guarantee flexibility in this matter. The most common acceptable reason is a demonstrable scheduling conflict with another course (which would imply that you are taking two courses that are scheduled at the same time). As an example, “Being able to catch a cheaper flight for a vacation” is not a suitable reason. Please alert us as soon as possible.